Analysis, Design and Implementation of High Speed Electrical Interconnects in Si VLSI

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The Problem: Interconnect delays have become the major limit in VLSI system speeds today. For high frequencies (in and above the GHz range on chip), on-chip electrical interconnect bandwidth is limited by the resistance, skin effect (AC resistance) of wires, capacitance, and dielectric dispersion of wires. [1, 2]. The speed of transistors in modern ICs increases substantially with every improving generation; however the raw, unbuffered speed of the electrical interconnect wiring increases slowly, limited by material, electrical and geometrical constraints. The intrinsic RC time constant of electrical wires stays approximately constant throughout process scaling; the l^2 dependence of the interconnect delay on the length, l, of the connection does not go away for smaller chips. In fact, since today's chips are becoming more complex, the average interconnect distance is actually increasing. As minimum wire widths and pitches decrease in more advanced technologies, wire heigths are increased to provide lower parasitic resistance, to increase current capacity and to reduce delays. However, this steep wire aspect ratio translates into greater mutual capacitance coupling between adjacent wires, increasing crosstalk noise. Simultaneous switching noise also increases due to faster signalling rates and increased complexity of modern ICs. Power supply distribution both on-chip and in chip packaging has become a major design issue in order to supply a low-impedance, low-inductance, and low-noise power supply to noisy digital circuits to prevent them from interfering with each other and causing bit errors. As chips operate faster, and at lower voltages, noise margins become ever harder to maintain.

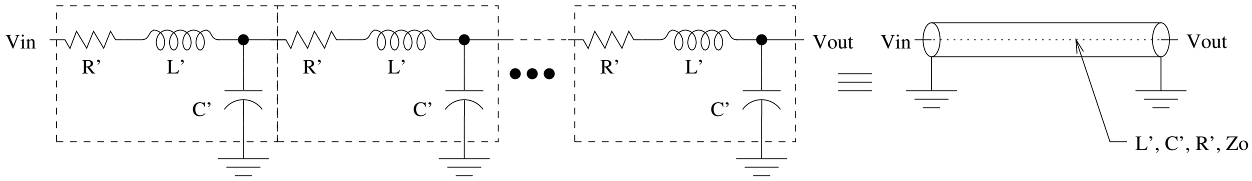
Motivation: A set of applications exists whereby a class of speed-critical signals (e.g. a pipeline stall signal in a microprocessor) need to be distributed globally, and the only thing that matters (next to power) is speed. since electrical interconnection delays have become the significant factor determining overall Si VLSI system speeds, new approaches for distributing high-speed, low-power, low-noise signals on and off chip must be developed [3].

Approach: Most researchers and industrial VLSI designers are relying only upon process improvements (e.g. low k dielectrics, copper interconnects, SOI technology, feature scaling, SiGe, etc.) to achieve performance gains needed for the next generation of VLSI technology. However, these improvements will only go so far, and more significant improvements can be obtained by a thorough investigation into the propagation mechanisms of signals on electrical wires, limitations on signal rates, and noise sources. Only then we can design the best circuits and electrical conduits which provide the greatest signalling rates at the lowest power and noise levels.

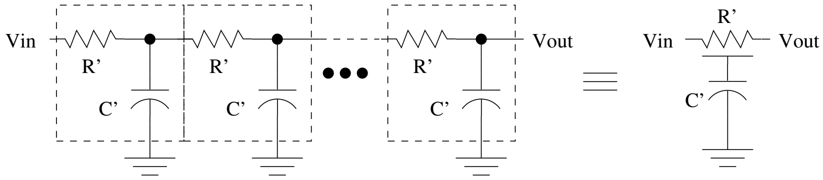
The traditional approach to sending high-speed signals across large distances on VLSI chips involves multiple high-current repeaters in a conventional CMOS design style [4]. New dynamic impedance circuits and low-noise, low-capacitance wire structures are being developed, which allow long RC-delay dominated signal lines across a chip to propagate at speeds much higher than simple repeatered lines, and with better signal integrity.

Figure 1 shows simple models for electrical interconnects. Electrical interconnects are divided into RC-dominated ($l < \frac{\lambda}{8}$, where l is the length of the wire, and λ is the wavelength), and transmission line or LC-dominated wires ($l > \frac{\lambda}{8}$). R', C' and L' are the per-unit-length resistance, capacitance, and inductance, respectively, of the wires. The transmission line shown has intrinsic impedance, Z_O.

A new differential regenerator circuit and on-chip differential transmission waveguide geometries are being combined to give rise to active impedance controlled lines with reduced voltage swings, suitable for high-speed and low-power communication across large chips. The combined effects of small, low-noise signal swings, differential signalling, and active guard-banding results in several orders of magnitude reduction in power consumption and between 10-100 times faster signal propagation compared to simple repeatered lines on chip. A differential-transimpedance receiver maintains constant voltage on each line segment, forcing the transmission line to operate in current mode (near constant



1. Uniform LCR Line and simplified schematic symbol



2. Uniform RC Line and simplified schematic symbol

Figure 1: Simple Models of Electrical Interconnections

voltage) effecting a "negative capacitance" and readily rejecting common-mode noise. The driver circuit is small – only large enough to supply the required communication current – in contrast to other voltage-mode drivers, which must worry about swinging large voltage signals on large capacitances in short time periods, wasting valuable power. The circuits are also designed to have high power supply rejection, PSRR, and low power supply noise generation, making them ideal for use in noisy digital environments, while operating off a single power supply, tolerating upto 20% VDD RMS noise. 10Gb/s signalling rates per line have easily been simulated in a TSMC 0.25μm technology. Actual circuits to be fabricated are expected to yield similar results.

Impact: Cleverly designed wires on chip and I/O pads off-chip will be able to carry information over 10 times faster in a given VLSI technology, without requiring special processing.

Future Work: Fab VLSI test chips; combine both source and line encoding for higher bitrates and clock recovery for off-chip interconnects.

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