Massachvsetts Institvte of Technology
Department of Electrical Engineering and Computer Science

6.313 Contemporary Computer Design

Problem Set #1 Fall, 1998, Due Wednesday 23 September

1. This problem concerns techniques for preventing the destruction of integrated circuits from high static voltage charges in the environment. When you walk across a rug on a dry day, your body accumulates a charge of several thousand volts. If you then touch electronic equipment, this stored energy must be discharged safely without destroying the electronics. We model your body as a 100 pF capacitor in series with 10,000 ohms, initially charged to a potential of 3000 volts.

(a) How much energy in the form of static electricity is stored in your body?

The input protection network of a modern integrated circuit consists of a conductive N+ doped silicon region above a P doped substrate. The N+/P region forms a diode, which, in normal circuit operation, is back biased, and effectively isolates the conductive N+ region from the substrate. The sheet resistance of the N+ stripe is 4 $ohm/\Box$. The protection circuit consists of a stripe 5 microns wide and 250 microns long in series with the logic input.

(b) What is the resistance of the N+ stripe?

The capacitance per unit area of the reverse biased diode is $CJ = 6 \times 10^{-4}\ F/m^2$, and the sidewall (perimeter) capacitance is $CJSW = 6 \times 10^{-11}\ F/m$.

(c) What is the total capacitance of the N+ stripe?

(d) What is approximate maximum signalling speed through this input protection device?

Joe Klutz now walks up and touches his finger to the input.
The N+ stripe quickly charges up to a sufficiently high potential (15 volts) that the N+/P diode junction breaks down, forming a conductor. The conductance of this layer in breakdown is $4 \times 10^{10}\ siemens/m^2$.

(e) What is the total conductance of the N+ wire to the substrate, assuming it is all in breakdown?

We now model the input protection structure as a distributed resistance conductance structure, with series resistance and shunt conductance.

(f) Define the resistance, R, and conductance, G, per unit length of the protection device and calculate their values.

(g) Derive governing differential equation for the distributed RG line in a way similar to the way we derived the equations for the RC and LC lines.

(h) What form do the solutions to this equation take?

(i) Describe why this protection structure is effective in preventing high voltages from appearing inside an integrated circuit.

(j) What problems do you anticipate as we scale these devices down to smaller dimensions and higher speed circuits?

2. Your engineering manager at Crayon Computer has asked you to design a test printed circuit board for the flagship Crayon-2000 processor product. Assume the dielectric constant of the board material is $K = 3.9$ and the relative permeability is $M = 1$.

The power required by the board is 100 amperes at 2.0 volts. You are required to bring this power into the board at one corner. The power is distributed on two power planes, each 2 ounce copper, separated by a 125 micron insulating layer. Assume that the current requirement is approximately uniform across the 20 cm x 20 cm board area.

(a) Estimate the voltage drop to the opposite corner of the board. I'm not interested in an exact solution. This is a tricky question, and you must make some assumptions to reach a solution. What assumptions?

(b) Calculate the capacitance between the power and ground planes on the board, assuming there are negligible cutout areas for component leads and via holes.

On the power plane side of the board, there is a 250 micron thick insulating layer topped with a 1/2 ounce copper conductive layer, which will be etched to form signal wiring, leaving the wiring exposed on the surface. This type of wiring is called microstrip wiring.

(c) The charasteristic impedence, Z, of a circuit is $\sqrt{LC}$. Charasteristic impedence is different from resistance; it gives the relation between V and I at a given point for a wave traveling along a perfect transmission line.

On the ground plane side of the board, there is a 250 micron thick insulating layer, a signal layer of 1/2 ounce copper, another 250 micron thick insulating layer, and finally a second solid copper ground plane at the surface. The transmission line structure formed in this way, with a signal wire surrounded on *both* sides with a ground plane is termed a stripline structure.

(d) Estimate the width of the copper wire which will have a characteristic impedance of 68 ohms.

(e) Estimate the signal propagation speed of this wire, in terms of fractions of c.

You have fabricated and tested your board,, but are now told that the board is to be run while immersed in deionized water, as a cooling material. (Bad idea).

(f) What are the impedances of the stripline and microstrip lines when the board is immersed?

(g) What are the speeds of propagation of the stripline and microstrip lines when the board is immersed?

3. Your company has just developed a high performance integrated circuit display device capable of fitting into your eyeglass frames. However, users report that the wire between the eyeglasses and the belt mounted computer system is annoying. You have been chartered to develop a wireless communications technique between the user's shoulders and the eyeglass frame.

You propose communicating between conductive shoulder mounted epaulettes (5 cm x 8 cm) and the metal rod of the user's eyeglass earpiece (2mm dia, 8 cm long). The glasses are separated from the epaulettes by a 12 cm air gap.

(a) Calculate the capacitance between the epaulette and eyeglass frame.

(b) You propose sending signals differentially between the left and right shoulder/eyeglass capacitors. To do so, you switch the voltage on the epaulettes from +5 to ground on one side, while simultaneously switching the signal from ground to +5 on the other side. The receiver circuit in the eyeglasses can be modelled as a capacitive 5 pF load. What is the expected magnitude of the voltage observed across the eyeglass rods with this capacitive load?

(c) Which aspects of this design will limit the maximum data rate achievable?

4. In class we derived that the RC delay of a wire was independent of the width. This is only true to a first order. Let's see what happens when perimeter capacitances are taken into account.

We have a signal that we need to transmit across our 10mm chip. The area capacitance of the wire is $80fF/u^2$ and the perimeter capacitance is $90fF/u$. The sheet resistance of the wire is 75 miliohms/square. Given the fixed 10mm length of our wire, the only parameter we have control over is the width.

(a) Plot RC delay for the wire as a function of width for widths between 1um and 10um.

So, within a certain range, you can affect the speed of your wire by varying the width.

(b) We drive our wire from 0 to 2.5 volts using a buffer, which can be modeled as a step input. The load at the end of our wire is a large gate which we can model as a 10pF capacitance. The energy required to charge a load with a step input is CV^2. How much energy is required to charge this load? Be sure to include the capacitance of the 10um wide wire in your calculation.

(c) What if this were a 32 bit bus running at 1MHz? How much power is consumed for 32 identical wires driving identical loads? ($Power = 1/2fCV^2$.) What percentage of the power is going to the wires? What percentage to the load?

(d) If the power budget for your chip is 5W, what percentage of your entire power budget is being spent in this 32 bit bus?