Massachvsetts Institvte of Technology
Department of Electrical Engineering and Computer Science

6.313 Contemporary Computer Design

Problem Set #1 Fall, 1998, Due Wednesday 23 September

Problem 1. 10 points

1a) $E = 1/2CV^2 = 4.5 * 10^{-4} J$.
A common mistake was to use the formula for power, which is different from energy (power = energy / time).

b) $250/5 = 50 squares => R = 50 * 4 = 200 ohms$.

c) $Csidewall * perimeter + Cjunction * area = 0.78pF$.

d) $t = (1/2)RC = 78 * 10^{-12} => maxfreq. = 1/t = 12.8GHz$.
$(1/2)RC$ is a better approximation for the time constant of a wire than RC. An intuitive explanation is that the *average* resistance from the input to a point on the wire that must be charged is $R/2$. (See text by Bakoglu.) However, I accepted those who used RC.

e) $4 * 10^{10} siemens/m^2 * 1250 * 10^{-12} m^2 = 50 siemens$.

f) $R/L = 0.8 * 10^6 Ohms/m$,
$G/L = 0.2 * 10^6 siemens/m$

g) The correct differential equation is:

```
 2
d V
--- = RGV  (R = resistance / length, G = conductance / length)
  2
dx
```

Note that this does *not* depend on time.

h) The solution to an order n differential equation has n degrees of freedom. The general solution to the above equation has *two* terms:

```
      -sqrt(RG)x      sqrt(RG)x
V = Ae             + Be
```

You need two constrains to solve for A, B. One constraint is obvious:
$V(0) = A + B$
The other constraint is not as obvious; it is a current constraint. Note that $I(x)R = -dV/dx$. We can make the reasonable assumption that $I(L) = 0$. Solving for A and B we find that B is more or less 0 and A is more or less

V(0) (So in this specific problem you end up with the right answer even if you forget to include the second term.. this is *not* true in general!)

i) The exponential falloff in voltage prevents high voltages from propogating across the structure.

j) Since RC stays the same, we could conceivably run into trouble if our speed starts to exceed 10GHz. Note that our regular input signals have to be able to pass through the input protection device unattenuated so that our circuit will function. We only want the bad, high voltage signals to be attenuated.

Problem 2. 6 points

2a) If we model the board as a wire with the same length ($20\sqrt{2}cm$) and area, we find a resistance per unit length of around $2 * 10^{-3} ohm/m$. A bad thing to do is to compute the voltage drop of 100mA flowing across this resistance. A better thing to do is to use the fact that the current is distributed. If R is the resistance/length and i is the current/length, we obtain the differential equation

```
 2
d V
--- = Ri
  2
dx
```

Solving using the constraints $V(0) = V0$ and $I(L) = 0$, we find $V(L) = V0 - (iL)(RL)/2$, so the voltage drop is half of what it would be if the entire 100mA flowed across the resistance.

b) $C = (K\epsilon_0 A)/h = 11nF$.

d) Microstrip:
$Z = h/w\sqrt{M/K}\sqrt{u_0/\epsilon_0} \Rightarrow w = 700um$.
Stripline:
capacitance doubles => inductance is halved => to get the same impedance the wire must be half as thick, so w = 350 um. Most of you figured out that capacitance doubles, but forgot about the change in inductance.

e) For both Microstrip and Stripline:
$v = c/\sqrt{MK} = c/2$.

f, g) For Stripline, nothing changes. The ground planes on all sides insulate the wire from any effect of the water.
Microstrip wires are difficult to evaluate. The approximation given in class is not valid as it assumed that the magnetic field lines are concentrated between the wire and the ground plane. When the board is immersed in water, this is no longer the case. Some of you tried to substitute K=80 for

water in the equation. However, most people were still using the $250um$ height for the insulator material which is *not* the height of the water.

Problem 3. 3 points

3a) $K = 1$ and $h >> w => C = (3/4)L\epsilon_0 = .53pF$.

b) The three capacitances are in series, so $1/Ceq = 1/C1+1/C2+1/C3 =>$ $Ceq = .25pF$ (roughly). Let V be the voltage across the 5pf load capacitor. By conservation of charge, $10 * Ceq = V * 5pf => V = .5$.

c) The resistance between the epaulettes and the load capacitance determines an RC time constant which will limit the data rate.

Problem 4. 4 points

4a) The RC delay is decreasing and non-linear. Here are sone points on the graph.

Width (um)	Delay (ns)
1	1950
2	1275
3	1050
4	937.5
5	870
6	825
7	792.9
8	768.8
9	750
10	735

(b) The load capacitor and the capacitance of the wire are in *parallel*. $Energy = (10pF + 9.8nF)(2.5)^2 = 61nJ$

(c) Total power $= 32(.5)(1MHz)(61nJ) = 0.99W$.
$C_{wire}/C_{Total} = 99\%$ to the wires.
$C_{load}/C_{Total} = 1\%$ to the loads.

(d) $0.99W/5W = 20\%$.