Massachvsetts Institvte of Technology
Department of Electrical Engineering and Computer Science

6.313 Contemporary Computer Design

Problem Set #2 Fall, 1998, Due Wednesday October 7

1. Your firm, American Telegraph, the respected telecommunications giant of the 1800's has just installed their new telegraph lines across the continent from New York to San Francisco. The wire communications path consists of a pair of #24 gauge (0.51 mm diameter) copper wire, held up on poles 8 meters above the ground and spaced 1 meter apart. The length of the run is 5000 Km.

(a) Calculate the parasitic resistance per unit length of the wire *pair*.

(b) Calculate the parasitic mutual capacitance per unit length between the conductors. Estimate rather than agonizing over solutions. Is this mutual capacitance the dominant capacitance in the circuit?

(c) Calculate the parasitic inductance per unit length of the wire pair. Estimate rather than agonizing over solutions.

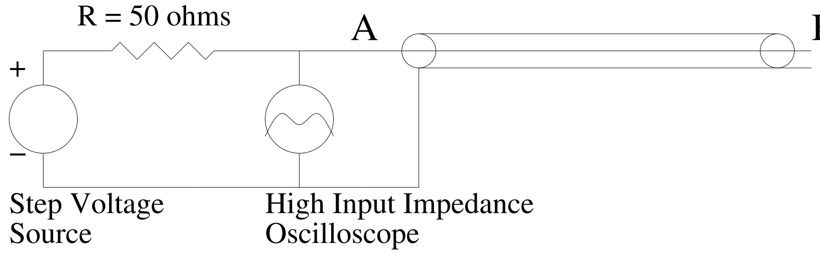
(d) Neglecting the resistance, what is the approximate (short haul) characteristic impedance of this line?

(e) You propose driving the New York end of the wire with a 100 volt voltage source in series with the telegraph key, and receiving it in San Francisco with a solenoid of 5000 ohm resistance, and negligible inductance. The solenoid requires 10 mA of current to close. Will your telegraph work? Why not?

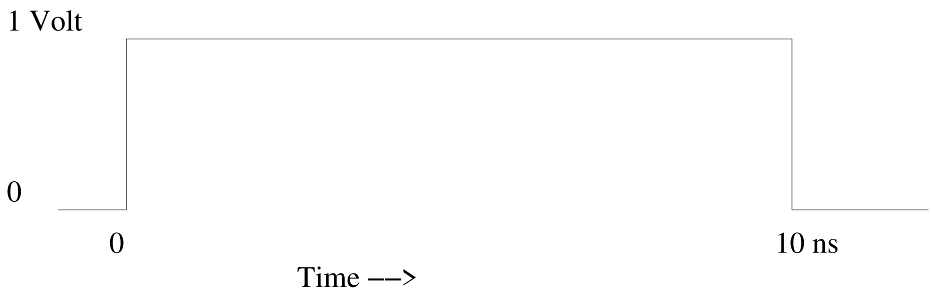
(f) Amplification to the rescue, you suppose: We'll just put a much more sensitive detector in San Francisco. You subcontract Western Electric to develop a detector with a 1 megohm input impedance and sensitive to 25 volt signals to place in San Francisco. Estimate the delay between when the key is closed in New York and the detector in San Francisco is activated. How many baud is your investment good for? Hint: Is this wire a capacitive, RC, or LC dominated wire?

(g) In disgust, your management almost contracts a Junior college on an fruit farm just south of San Francisco to redesign your system, but gives you one more chance to salvage their massive investment of hundreds of thousands of dollars in wire and right of way. What changes do you recommend to either the signalling system at the end points or modifications you can make or devices you can add along the wire run which will avoid having to remove and restring the wiring, while still increasing the signalling rate?

2. Your oral exam committee gives you one end (A) of a transmission line, which is connected to a time domain reflectometer (1 volt step voltage source, resistor, and oscilloscope as shown below). The committee keeps the other end of the line (B) hidden from you under the table.



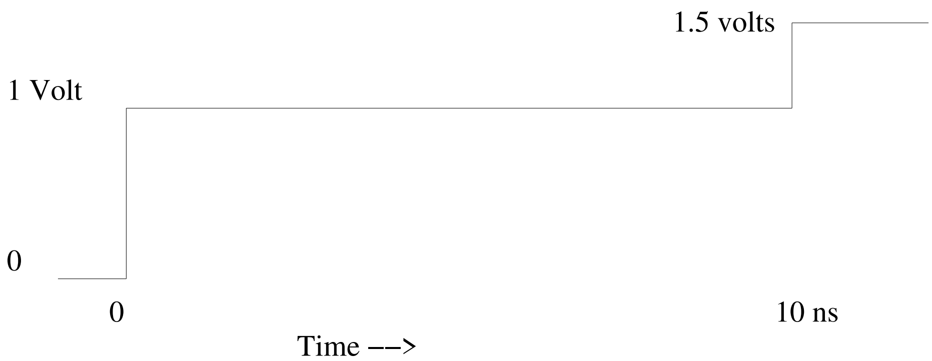
Before the exam starts, you observe the following trace on the TDR:



You are told that the line is made of copper, and insulators have $K = 4$, and $M = 1$.

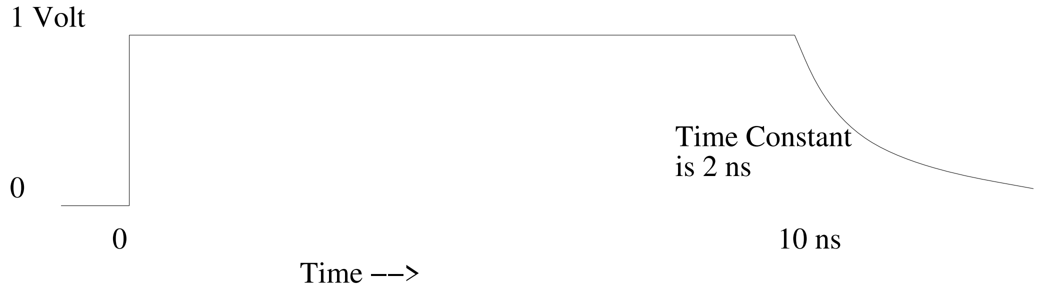
(a) What conclusions can you draw about the line impedance, delay of the line, length of the line and the condition of the end of the line from the above trace?

Inquisitioner #1 announces that he has brought a fine red device which can be modelled as a single passive circuit element and would like you to identify it. He fiddles for a minute under the table, connecting the device to the end of the line, and the trace changes as shown below:



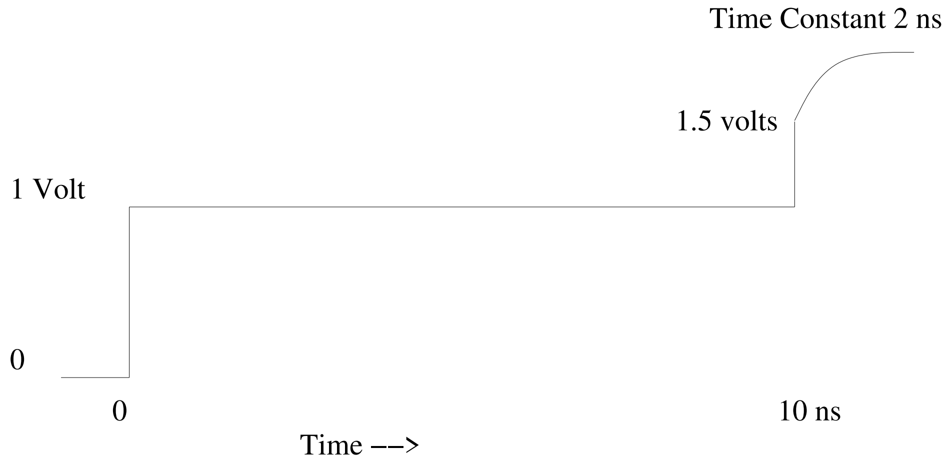
(b) He asks you to draw (with component values) the simplest model of what he has attached to the end of the line consistent with the evidence you have.

Inquisitioner #2 similarly announces that she has brought a most excellent blue device, fiddles for a minute under the table, and the trace changes as shown below:



(c) Again, she asks you to make a model of the single device, but also, to draw the voltage waveform with respect to time for the point at the end of the transmission line.

Inquisitioner #3, not to be outdone, brings out *two* fine, gold plated black boxes, and expertly connects them to the end of the line with a *take that* gesture. You observe the follow trace:



(d) He asks you to make a plausible model for the pair of devices, their values, and of how they might be hooked up.

3. The SIMM memory array on your Wintel computer motherboard consists of an 18 cm long wire connecting six sockets, equally spaced every 3

cm along the wire, and terminated at the far end with a resistor located 1.5 cm from the last socket. The driver is located 1.5 cm away from the first socket. The impedance of the line is measured, without SIMMs, to be 50 ohms. The speed of propagation is measured, again, without SIMMs, at $c/3$.
Throughout this problem, we will assume that the signals travelling have risetimes such that the propagation between card slots is small compared to that risetime, which allows us to treat the load capacitances as distributed capacitances.

(a) What is the total capacitance of the line (without SIMMs)?

(b) What is the line capacitance per centimeter and the line inductance per centimeter for the line (without SIMMs).

Into each slot, we now plug a SIMM containing a 2 cm long copper trace connected to a memory component which we model as an 8 pf load capacitor. The copper trace is 200 μm wide, and 100 μm above the ground plane.

(c) Estimate the capacitance of the 2 cm long copper trace on the card.

(d) Recalculate the total capacitance per centimeter of the motherboard bus, including the the original capacitance from part (a), the 2 cm card capacitance, and the 8 pf driver/receiver capacitance. Assume that, because of the speeds involved, the SIMM capacitance can be effectively spread out uniformly along the motherboard wire.

(e) Recalculate the line impedance of the bus with the capacitive load from all of the cards present. To what values should I change the resistor at the end of the line as a result of plugging in the cards?

(f) Recalculate the speed of propagation of the bus signals with the capacitive load from all of the cards present.

4. You are hired to perform an important field modification to a high speed ECL system, which uses controlled impedance stripline wiring for all of its interconnections. The board and backplane impedance for all wiring is 60 ohms, and all terminations are parallel, 60 ohm terminations at the receiving (non driven) ends of all lines.

In particular, the modification you wish to make concerns the output of a logic gate on board A, which drives one end of a line, travels over the backplane to board B, drives the input to a logic gate and is terminated there.

The modification requires you to connect this signal to a gate located on yet another board, board C. Unfortunately, there are no spare connector pins on either board A or B, and only a single spare pin on board C (ground return pins are available on all the boards). You must improvise. The wire you are given to make the repair is twisted pair, with a characeristic impedance of 120 ohms. Also available is an unlimited supply of 60 ohm resistors. Describe how you might use the twisted pair and resistors to replace or augment the existing wiring to connect the signal on board A (also available on the backplane) to both boards B and C. The network you build must be terminated so that no reflections occur. Both the logic inputs on boards B and C must receive full swing inputs.

There are at least two good solutions. Specify if and where the ground pins on the twisted pair are connected, as well as the signal pins. You have access to the component and connector pins on all boards and (if necessary) may disconnect them from the PC board traces already present.