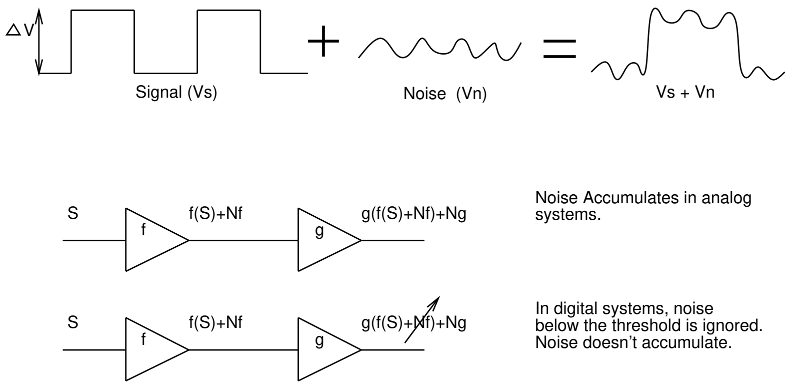


Figure 1: Noise in analog and digital circuits.

6.915 Digital Systems Engineering - 09/16/96

Noise: "The Hard Problem"

1 Noise

The main difference between analog and digital systems is how they handle noise. In analog systems, noise accumulates and cannot be removed. In digital systems, noise can be completely removed (the original signal "regenerated") if the amount of noise is below a threshold.

To provide the largest noise margins, the switching threshold of digital circuits should be $\Delta V \div 2$, where ΔV is the difference between the voltage levels for a '1' and '0'. Note that for a digital circuit to function correctly, $V_N < \Delta V \div 2$.

An example of a single-ended voltage level signalling is provided by TTL (Transistor-Transistor Logic). Noise margins are the difference between the worst valid output level, and the worst acceptable input level. The forbidden zone represents voltage levels where the circuit behaves as an analog amplifier, and does not produce valid output voltage levels. Sensitivity is defined as the range of input voltages corresponding to the forbidden zone (the smaller the sensitivity, the better).

Noise can be divided depending on sources: $V_N = V_{NI} + k_N \Delta V$. V_{NI} represents fixed noise, such as shot noise, etc. The other term is noise proportional to other voltages or changes in voltages in the system. Proportional noise is also referred to as 'interference'.

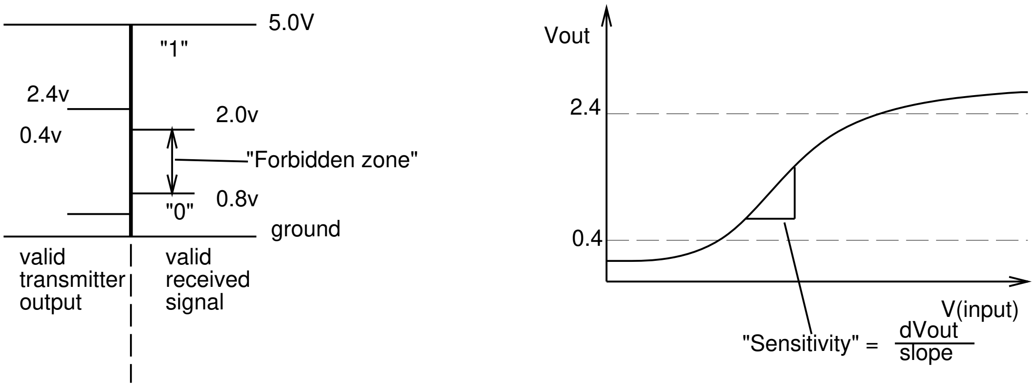
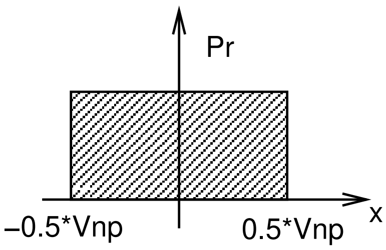
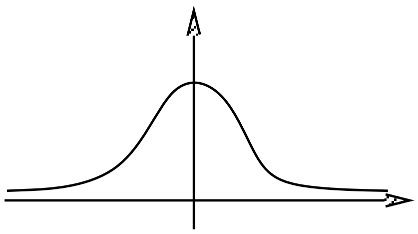


Figure 2: Valid TTL output/input levels, with noise margins and forbidden zone.



Magnitude of noise from bounded source.



Unbounded source: gaussian distribution

To improve the sensitivity of a receiver, we can create V_r, an estimate of the amount of noise in a signal. Then, the voltage seen by the receiver is: $V_R = V_S + (V_N - V_R)$. The term $(V_N - V_R)$ is the amount of uncancelled noise remaining in the received signal.

2 Worst-Case Design

There are two kinds of noise sources: bounded and unbounded.

Some sources of Gaussian noise:

- Johnson noise from resistors. Usually in the microvolt range, generally not a problem in digital systems.
- Coupling to other signals. Usually the coupling effects of many signals tends to average out, but sometimes a large number of signals will switch in exactly the wrong pattern. Example: a 64-bit bus going from 0's to 1's.
- Alpha particle hits. Not really Gaussian (either it misses, or you're hosed).

3 Voltage Noise

Figure 3 shows a model for noise in a voltage-level signal system. There are many sources of noise, and they all add up. Use of a reference (return) line is a significant improvement over single-ended signalling (using the lower 'ground' wire as reference).

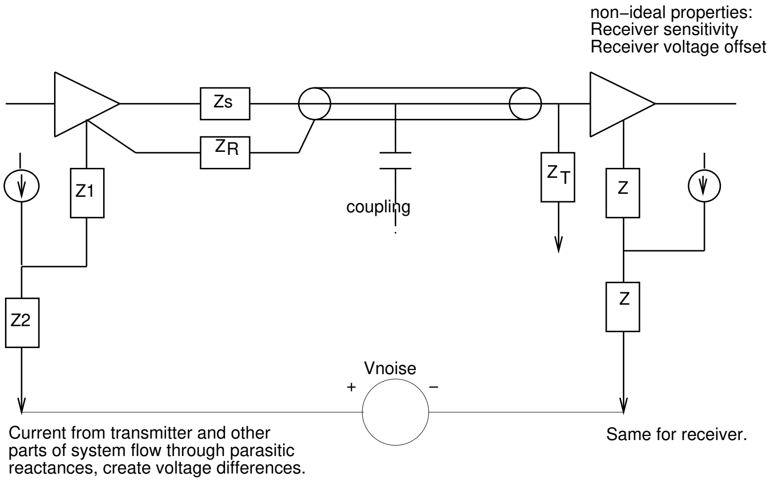


Figure 3: Model for voltage noise in voltage-level signalling system.

4 Timing Noise

Timing noise is uncertainty in the timing of signals. Many systems depend on predictable time behavior (delays) of their elements. Sources of timing noise are:

- Intrinsic: Thermal noise of oscillators. Small, except in some critical circuits. Usually ignore.
- Noise + Nonzero edge times: Especially when signals have long edge times, a small amount of noise can change the time when the signal crosses the switching threshold. $T_N = V_N \div slope$.
- Delay through logic gates changes with respect to supply voltage. The higher the supply voltage, the faster a CMOS circuit switches. If part of a chip experiences IR power drops, its delay increases. Because of the complexities of power distribution (inductance to package, IR drops, etc.), different parts of a chip may see different power supply values, and have different delay characteristics.

5 Power Suply Noise

Inductance of packaging limits the rate of change of power supply current of a chip. Switching of large devices creates current spikes, which result in voltage drops. In addition, V=IR voltage drops are becoming very significant as chips become smaller.

Typical values: two adjacent circuits on a chip: 10mV power supply difference; across a chip: 300mV.

6 Models

Single-ended signals are implicitly referenced to system ground. The problem is that 'ground' may refer to different potentials in different locations.

Use of an explicit reference signal can greatly reduce the effects of noise on a receiver. However, this approach increases the number of wires necessary to transmit a signal. A reference signal can be shared by multiple receivers, however this sharing will degrade performance.

And finally, current-mode signalling can do even better. Output resistance of transmitter should be high (current source), and input resistance of receiver should be low. Noise voltages are reduced by the ratio of these resistances.

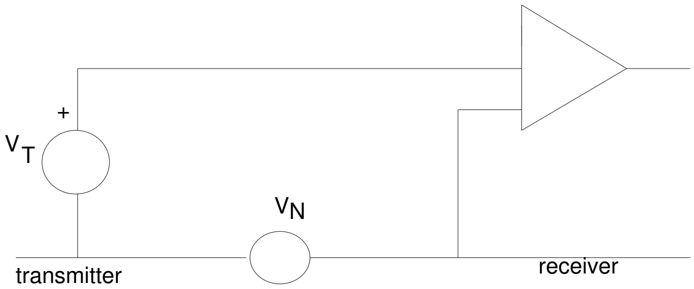


Figure 4: Single-ended system with ground noise.

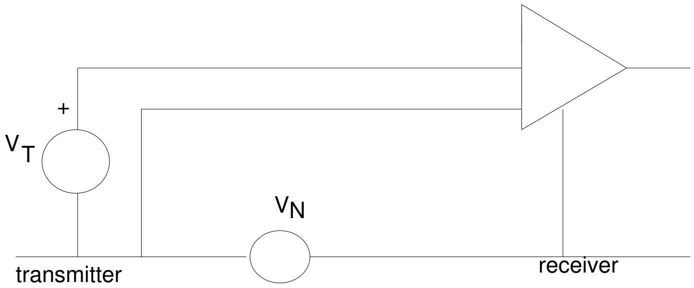


Figure 5: Differential system is less affected by power supply noise.

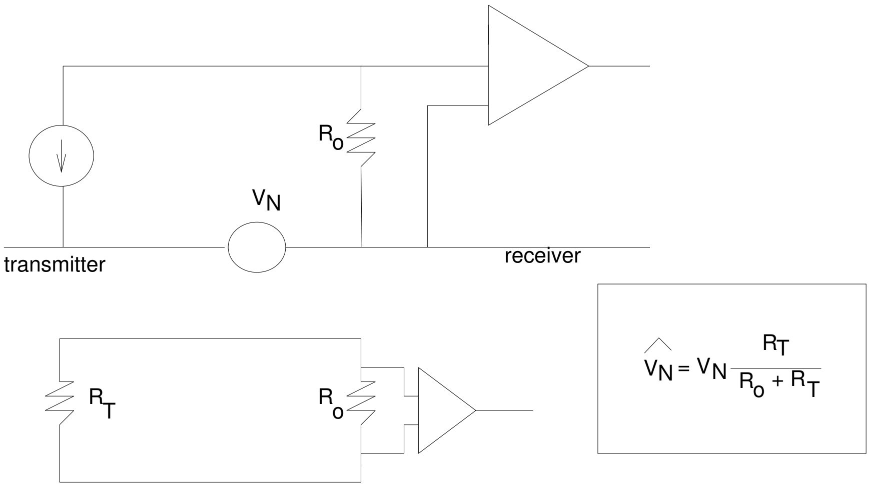


Figure 6: Current-mode signalling.

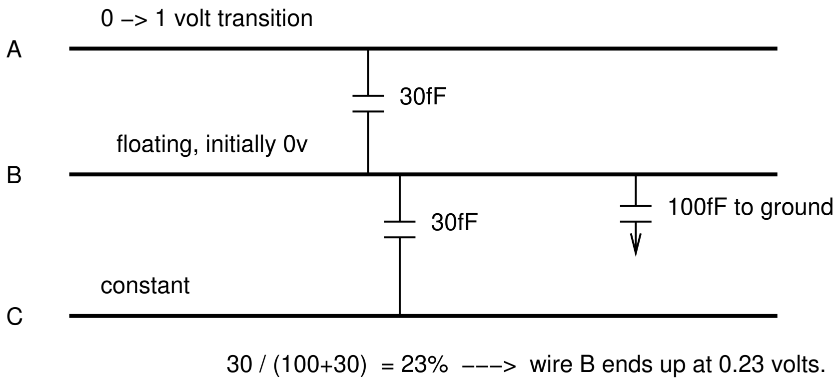
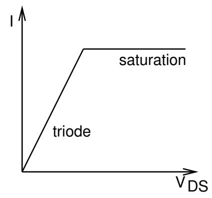


Figure 7: Crosstalk due to coupling capacitances.



7 Crosstalk

Crosstalk is the interference of a signal on one line with a signal on another. The moral of the story is that floating nodes are a bad idea.

Coupling capacitances are increasing as minimum feature size on chips becomes smaller. Values typical of modern 0.35um processes: 0.05fF/um between a metal wire and the layer below it; 0.03fF/um between a metal wire and a minimum-spaced wire adjacent to it.

Solution to coupling noise: **No long floating wires!**

But even when wires are driven, coupling capacitance affects switching characteristics. Depending on what the adjacent signals are doing (constant, transition up, transition down), a signal's rise time can vary greatly. Large voltage spikes due to coupling can cause a receiver to see an incorrect value. Example: domino logic.

8 Do's and Don'ts

- Have a set of ground rules to prevent common problems.
- When possible, don't use floating signal lines.
- Use the slowest edge rate (longest edge time) allowable.
- For critical nodes, use shielding and/or filtering (e.g. LPF for DC bias voltages).

9 MOS Transistor model for digital designs

For small drain-source voltages, it looks like a resistor. For large drain-source voltages, it looks like a current source. Simple, isn't it?

09/19/96 achen