Chapter 1

Electrical Behavior of Wiring

1.1 Motivation

This chapter presents material which should be familiar to you, although it is presented with a different emphasis than you may have previously encountered. The emphasis here is on the relationship between the physical structure of circuit components and the electrical behavior of the elements. In particular, we analyze in detail the structure and properties of electronic interconnect. Wires are the most expensive components in modern digital designs whether measured in dollars, performance impact, size, or design cost. Yet our most common circuit models make the very questionable assumption that wires cost nothing and are parasitic free. For high speed digital design, wires now are responsible for more than half of the circuit delay, and must be treated as components in their own right. This chapter begins to address this issue by properly analyzing the wire as a component. First, we consider the individual parasitic component behavior of wire by discussing resistance, capacitance, and inductance. We then address the more complex issues arising when wires are operated at very high frequencies, when more than one such parasitic element is important. We pay particular attention to the scaling behavior of wiring and to the practical and theoretical reduction of parasitics.

1.2 Resistance

The DC behavior of wiring is largely governed by the wire resistance. A cross section of our prototypical wire is shown in figure 1.1 with width w, thickness t, and length l. Also shown is a current return path, called a *ground plane*, which acts both as a reference plane for capacitive and inductive effects, and as a return current path. The ground plane is separated from the wire conductor by a height h.

The end to end resistance of the wire is given by the formula:

$$R = \rho \frac{l}{wt}. \tag{1.1}$$

Where ρ is the material resistivity of the conductor, measured in ohm-meters.

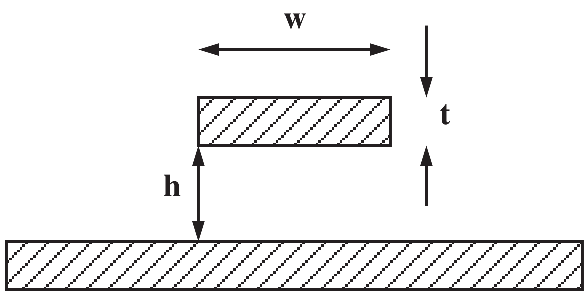

Figure 1.1: Prototypical Wire and Groundplane Dimensions

In common with other wire parasitics, the resistance depends on a *material property*, ρ, and on a *geometric factor*, l/wt.

1.2.1 Resistance Rises with Device Shrinks

When all dimensions of a conductor shrink by some constant scale factor k, the scaled resistance

$$R' = \rho \frac{l/k}{(w/k)(t/k)} = \rho \frac{lk}{wt} = kR \tag{1.2}$$

of the conductor goes up by a factor of k. This simple result tells us that parasitic resistances are increasingly important as we scale to smaller circuits.

This *scaling behavior* of wire and other devices is a major concern in modern electronics, because it directly controls the performance of circuits as we scale the physical dimensions of system to smaller sizes. Strong economic and performance motivations encourage these size reductions, but parasitics such as line resistance limit the performance improvement available. Because of the importance of scaling, we will discuss its implications throughout the text.

1.2.2 Resistivity

Electronic materials are characterized by their *resistivity*, ρ, measured in units of ohm-meters. Table 1.1 gives the resistivities of some common electronic conductors along with their temperature coefficients. These resistivity values correspond to the resistance between the opposite faces of a cube of the material one meter on a side. Material property values are sometimes given as *conductivity*, σ, the inverse of resistivity. The units of conductivity are siemens/meter, sometimes denoted in older texts as mhos/meter.

Material	Resistivity $\times 10^{-8}\ ohm \cdot m$	$\Delta R/R$ per K	Density $\times 10^{6}\ g/m^{3}$
Aluminum	2.824	.0039	2.70
Beryllium	2.65		
Brass	7	.002	8.6
Chromium	20		
Constantan	49	.00001	8.9
Copper, annealed	1.7241	.00393	8.89
Copper, hard drawn	1.771	.00382	8.89
Copper Tungsten 20-80	2.5		
Copper Molyb. 20-80	2.4		
Gold	2.44	.0004	19.3
Iron, .9998 pure	9.71	.005	7.8
Lead	20.64	.0039	11.4
Solder, 50-50	15		8.89
Solder, 95-5	19		10.9
Magnesium	4.45	.004	1.74
Mercury	95.783	.00089	13.546
Molybdenum	5.34	.004	9.0
Nichrome	100	.0004	8.2
Nickel	6.84	.006	8.9
Palladium	10.8		
Platinum	10.6	.003	21.4
Silver	1.59	.0038	10.5
Steel, Carbon SAE 1020	10		7.86
Steel, Stainless 304	72		8.02
Tantalum	15.8	.0031	10.0
Tin	11.0	.0042	7.3
Tungsten	5.4	.0045	10
Zinc	5.964	.0037	7.1

Table 1.1: Table of Conductor Resistivities

The extremely wide range of material resistivities, ranging over twenty orders of magnitude is a major reason for the relative ease of designing electronic structures. Crudely, we characterize electronic materials into one of three classes, depending on their resistivities: *conductors*, with $\rho < .1$ ohm-meters; *semiconductors*, with $.1 < \rho < 100$ ohm-meters; and *insulators*, with $\rho > 100$ ohm-meters.

The most conductive material at room temperature is silver, followed closely by copper. Economic factors dictate the widespread use of copper, although silver finds some applications in plating of copper wires and in microwave equipment to control skin effect losses. In microelectronic applications, the dominant wiring is aluminum, with the occasional use of gold metallization. As resistive scaling effects begin to dominate performance at small dimensions, process engineers are beginning to consider the use of copper metallization despite its processing difficulties.

1.2.3 Impurities Increase Resistivity

Pure materials tend to have a very much lower resistivity than even slightly impure materials of nearly the same composition. Thus, copper which has been alloyed with even small amounts of other metals has dramatically higher resistivity than pure copper. Brass, for example, is a relatively poor metallic conductor.

The mechanical handling of materials can also influence their resistivity. Work hardened copper wire, for example, has a slightly higher resistance than a similar heat annealed copper wire.

1.2.4 Low Temperature Reduces Resistivity

In general, the resistivity of conductors decreases approximately linearly with the absolute temperature. Copper, for example, decreases in resistivity by about a factor of four at liquid nitrogen temperatures. Figure 1.2 shows the resistivity of copper versus absolute temperature.

Example:

> A computer power supply must be connected to a remote processor. Calculate the required diameter and wire gauge of a 1 meter copper power wire delivering 200 amperes of +1 volt DC power with less than a 2% voltage drop.

Solution:

> The current travelling toward the computer must also return – hence the loop length is two meters. The resistance of such a wire is $R =$

Figure 1.2: Plot of Copper Resistivity vs. Absolute Temperature

$\rho l/\pi r^2$, where r is the radius. We require a resistance $R < V/I = .02/200 = 10^{-4}$ ohms. Solving for r,

$$r = \sqrt{\frac{\rho l}{\pi R}} = \sqrt{\frac{(1.72 \times 10^{-8}\ ohm - m)(2\ m)}{(3.14)(10^{-4}\ ohm)}} = 10.5\ mm. \qquad (1.3)$$

The minimum required diameter is 2.1 centimeters. Welding cable does not ordinarily come in sizes this large, so multiple wires or machined copper bus bars will be required.

1.2.5 Sheet Resistance

In working with many fabrication processes, such as semiconductors and printed circuits, the thickness of available conductive layers is a manufacturing process constant, set by the manufacturing engineer, and not readily under the control of circuit engineers. It then makes sense to compute wire resistances on the basis of width, w, and length, l, factoring the material resistivity, ρ, and the material thickness, t, into a process parameter termed the *sheet resistance*. The sheet resistance, R_s, has units of $ohm/\square$, representing the resistance of one square of the material, although the square is unitless. The sheet resistance is given by:

$$R_s = \rho/t. \qquad (1.4)$$

The utility of sheet resistance as a concept is evident from figure 1.3 , where the resistance of the wire can be calculated by counting squares of material. Equivalent resistances of complex geometries can be evaluated by breaking the geometry into finer squares.

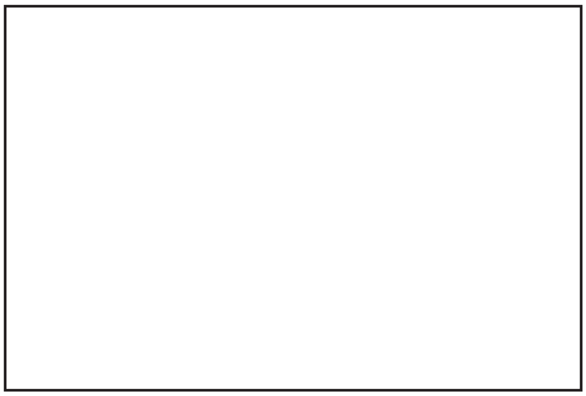

Figure 1.3: Measuring the Resistance of Sheets by Counting Squares

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Example:

> A printed circuit board is clad in 1 ounce copper. Calculate the sheet resistance, and the DC resistance of a 10 cm trace which is 1 mm wide.

Solution:

> Common U.S. industrial practice denotes a copper layer as one ounce when a square foot of board is coated with a copper layer weighing 1 ounce. The density of copper is 8.89 g/cm^3, so one ounce (28.37 g) of copper has a volume of 3.19 cm^3. One square foot has an area of 30.48×30.48 or 929 cm^2, so the thickness of the copper layer is 34.4 μm. The sheet resistance is then $R_s = \rho/t = 1.72 \times 10^{-8}\ ohm-m/34.4\ \mu m = 5.02 \times 10^{-4}\ ohms$. The wire consists of 100 squares, so the wire resistance is .05 $ohms$.

Example:

> The Digital Alpha 21064 microprocessor has a 1 μm wide aluminum metal-1 wire travelling the length of the 16.8 mm die. The sheet resistance of the metal-1 layer is .04 $ohms$.
> (a) Calculate the approximate thickness of the aluminum layer.
> (b) Calculate the DC resistance of this wire.
> (c) The chip now undergoes a linear shrink by a factor of two in all three dimensions. Calculate the resistance of the wire in the smaller chip.

Solution:

(a) $t = \rho/R_s = (2.8 \times 10^{-8})\ ohm - m/(.04\ ohm) = 0.7\ \mu m$
(b) The wire is $16,800\ \mu m$, and hence 16,800 squares long. The resistance is $(16800)(.04) = 672\ ohms$.
(c) A linear factor of two shrink in all three dimensions will raise the sheet resistance by a factor two, and raise the resistance of the wire by a factor of two. A more desirable shrink, from a circuit design perspective, would shrink in width and length, keeping the thickness and thus the sheet resistance constant, resulting in unchanged resistance. These non-uniform shrinks are extremely difficult to achieve in modern processes due to difficulties in etching and step coverage of thick metal layers. Wires in a typical modern semiconductor process are comparable in thickness to their minimum width.

Problem:

The concept of sheet resistance outlined in the text is useful in evaluating the resistance of straight wires in a simple way. Wires with 90^o bends, however, exhibit *current crowding* in which the major portion of the current flows in the inner portion of the bend. Derive a rule of thumb for evaluating the effective resistance of wires with 90^o bends in them, by splitting such a bent wire into resistive squares, forming a mesh of resistors, and solving for the effective resistance of a corner square of resistive material. In counting squares of resistance, how many squares should we count for the square at the corner?

Solution:

Solution goes here.

1.2.6 V-I Characteristics of Resistors

Recall that the relationship between current and voltage in a resistive circuit is approximated by the linear relationship Ohm's law,

$$v = iR. \tag{1.5}$$

This relationship is valid only for voltages and currents which are neither too large nor small, but is a useful approximation for most materials under common operating conditions. At low voltage and current, the discreteness of charge carriers must be considered. At high voltage and current, dielectric breakdown, conductor self-heating, and fusing introduce marked temporary nonlinearities and permanent device changes.

1.2.7 Power dissipation in Resistors

A resistor converts electrical into thermal energy. The energy per unit time, or power converted is given by

$$P = iv = v^2/R = i^2R. \tag{1.6}$$

This heat must be removed from systems, and constitutes a major reliability issue in large system design. Resistive losses in well designed wiring are typically a small source of power dissipation in digital systems. Careless design, however, can lead to localized hot spots and reliability defects such as electromigration. Although not a significant source of power dissipation, the resistance of interconnect wiring has a first order effect on the speed of digital systems.

1.2.8 Electromigration and Maximum Current Densities

The heat dissipated in resistive interconnect causes atoms in the wiring to move more rapidly. These faster moving atoms are more mobile, and can migrate from regions of high current density, and thus higher temperature, to other regions of the conductor. This results in a reduced area conductor in the high current density areas, further increasing the current density. A runaway situation results, called *electromigration*, where the conductor eventually acts as a fuse, opening the circuit.

This thermally generated electromigration can occur over ten year intervals, and is a significant cause of long term failure of microelectronic devices. Especially sensitive areas include corners, where current crowding increases the local current density, and at inter-layer interconnect contacts and vias, where the available material at the contact may be significantly smaller than in straight wire runs.

Approximate limits for maximum DC current density of aluminum interconnect are 1 $mA/\mu m^2$, or for current generation circuits, assuming a required lifetime of 100,000 hours and a maximum die temperature of 125^oC. For current generation circuits with 0.5 μm thick metal wiring, we require a 2 μm wide line to support 1 mA of current. Although these current limitations do not present major difficulties in design, careless layout can easily result in circuits for which these limits are exceeded.

Electromigration is controlled in commercial microelectronic circuitry by limiting the maximum current density of interconnecting wires, and by controlling substrate temperatures. Fortunately, silicon and metals are excellent thermal conductors, and at small dimensions the relatively high thermal resistance of insulating oxide is a small effect. Liquid nitrogen cooling of microelectronic circuits effectively eliminates the long term electromigration reliability issues.

Recent evidence shows that the maximum allowable current density in a wire is strongly dependent on whether the current flow is AC or DC. AC current flow induces electromigration failures at a rate up to ten time slower than corresponding DC flow.

1.2.9 Scaling of Electromigration Limits

Current density of interconnect wiring scales up with the scale factor k in a way similar to line resistance. Its importance as a design limitation will increase with the design of smaller devices.

1.2.10 Matching of Resistor Values

The control of absolute resistor values in modern integrated circuit processes is typically very poor, with values varying by more than a factor of two from manufacturing lot to lot. Circuit design techniques have evolved over the past thirty years to rely less on the absolute value of the resistive components, and more on the ability of modern manufacturing processes to produce components which are matched in their behavior. Although an integrated circuit process cannot typically produce a resistor whose value is known to 5% tolerance, it can easily produce *two or more* resistors whose values are the *same* within a 5% tolerance.

The basic strategy for fabricating matched resistors is to construct devices which are physically similar, with the same geometry, orientation, and direction of current flow. There are important effects, however, in integrated circuit manufacturing, which limit the matching of silicided active area wiring and polysilicon resistors, notably the presence of grain boundaries. Near minimum width wiring can exhibit factor of ten differences in resistance when the grain size is of the same order as the width of the wiring. Care must be used in the layout and circuit process to eliminate dependence on such resistor value matching, even when the structures designed are matched in geometry and orientation.

1.2.11 Superconductors

When sufficiently cooled, some materials, the *superconductors*, exhibit a total loss of DC resistance. First observed in metals in the early 1900's, this effect required cooling to liquid helium temperatures (4.2^oK). Material research gradually raised the critical temperature for conventional metallic superconductors to about 20^oK, which remained the upper limit for many years. In 1987, a new class of ceramic copper-metal oxide superconductors were discovered, dramatically raising the transition temperature above 100^oK. The high transition temperature of these material allows the use of much less costly liquid nitrogen cooling (77^oK). Unfortunately, these ceramic materials remain difficult to fabricate and work with in forms suitable for microelectronic applications. One notable difference between the metallic and oxide superconductors is the highly anisotropic behavior of the copper oxide based materials, preferentially conducting in two crystal axes much more readily than in the third.

The total absence of DC resistance is the striking property of superconducting materials. This superconducting effect is quenched, however, in high magnetic fields. This field sensitivity includes fields which are generated by current flowing through the superconducting wire itself. This self-generated field quenching limits the maximum current density of superconducting wires to relatively low levels of about $100,000\ A/cm^2$ or $1\ mA/\mu m^2$. Power distribution inside of microelectronic systems, otherwise an excellent application for superconductors, is highly constrained by this current density limit, which is similar in magnitude to the limit for electromigration in aluminum lines.

The zero resistance wiring which may eventually be possible with superconducting films could eliminate some difficult wiring problems, both in the power distribution and in the high speed propagation of signals on long wires, but this promise has yet to be realized due to the intractable materials issues.

1.2.12 AC Resistance and the Skin Effect

Until now, we have discussed in this chapter the behavior of electrical conductors carrying DC current. Several aspects of electrical conduction change when we consider the ability of conductors to carry AC waveforms. In particular, a frequency dependent resistance, termed the *skin effect* becomes an important parasitic.

AC signals travelling through a wire generate a time varying magnetic field. This field in turn produces eddy currents in the conducting wire, which effectively balance the generated magnetic field. For perfect conductors, the induced eddy currents exactly balance the field, preventing field penetration into the conductor, and current flows only in the surface layer of the conductor. For resistive conductors, the resistance reduces the eddy current formation and prevents complete balancing of the field. Penetration of the magnetic field into the conductor occurs, falling off exponentially at greater depths with the conductor. Conduction through the wire is limited to this surface region, where partial penetration of the wire by the induced magnetic field occurs.

We can approximate the resulting resistance as being due to a surface *skin* of conductive material of depth δ, given by

$$\delta = \sqrt{\frac{\rho}{\pi f M \mu_0}}, \tag{1.7}$$

where μ_0 is the permeability of free space, M is the relative permeability of the surrounding materials, ρ is the material resistivity, and f is the signal frequency. At a depth of δ, the field penetration has dropped by a factor of $1/e$.

An aluminum wire, at $f = 1$ gigahertz, for example, has a skin depth of 4 μm and an effective surface sheet resistance of 0.028 $ohms/\square$. This sheet resistance is comparable to the DC sheet resistance of the wiring.

Note that the frequency variable component of this behavior reduces the conductivity of wiring for high frequency signals, effectively making the surface properties the only properties of significance. The common use of silver plating in high frequency digital and microwave circuits capitalizes on this behavior to achieve the effective conductivity of silver interconnect at the cost of base metal supports.

The surface roughness of conductors at high frequency is also important. Highly polished surfaces are used in microwave equipment to minimize the conductive path length at the scale of the skin depth. 1 μm surface bumps can add significant surface sheet resistance to signals of 10 gigahertz.

For integrated systems, the skin effect plays a major role, making the already problematic resistance of metal wiring even more difficult to deal with for high frequency signals.

Material	Penetration Depth $\delta(m)$	Surface Resistance $R_s(ohm/\square)$
Aluminum	$.0826/\sqrt{f}$	$3.26 \times 10^{-7}\sqrt{f}$
Copper	$.0660/\sqrt{f}$	$2.61 \times 10^{-7}\sqrt{f}$
Silver	$.0642/\sqrt{f}$	$2.52 \times 10^{-7}\sqrt{f}$

Table 1.2: Table of Skin Depth and Surface Resistance

1.2.13 Insulators

Our ability to effectively isolate one portion of a circuit from another is just as important as our ability to connect nodes together. *Insulators* are materials which exhibit very low DC conductivity, and which can be used for this isolating function. Surprisingly, the material properties of insulators also play a major role in the design of microelectronic systems. For DC systems, the most important insulator property (other than its resistivity) is the *breakdown field strength*, which determines the maximum sustained electric field across the material without inducing breakdown. We normally associate *dielectric breakdown* with lightning storms, but even low voltages, combined with the small dimensions of modern integrated circuits, can result in dielectric breakdown. The breakdown field strength of several widely used insulators is shown in table 1.3.

Example:

Calculate the electric field between the gate and channel of a modern MOS transistor with a gate oxide thickness of 7 nm and an applied gate to source potential of 1 volt.

Solution:

$E = v/t = (1)/(7 \times 10^-9) = 1.4 \times 10^8$ volts/meter. This is sufficiently below the breakdown field strength for silicon dioxide, allowing the use of the dielectric as a gate oxide.

The electric field is partially determined by the geometry of the electrodes. Sharp points, in particular, result in high field strengths near the points. Thus, high voltage circuitry traditionally is designed with smooth, spherical electrodes. Similar techniques are sometimes used to eliminate sharp points in critical circuits of modern integrated circuits, notably in the *input protection* devices, where we often find the only circular or rounded corner devices in a design.

1.2.14 Electron Tunnelling limits Minimum Insulator Thickness

1.3 Capacitance

The second important parasitic in interconnect wiring is the *capacitance*. A capacitor consists of two conducting electrodes separated by a dielectric material. Capacitance is an important wire property because a signal travelling through a capacitive line uses energy to charge the line prior to the signal proceeding further down the line. The capacitance thus partly controls the speed of propagation of signals on the line.

We can derive the capacitance of a parallel plate structure shown in figure 1.1 by considering the current voltage relationship. We assume in this discussion that h is small compared with w. An applied voltage v results in an electric field $\mathbf{E}$ of magnitude v/h volts/meter. The displacement field is given by

$$\mathbf{D} = K\epsilon_0\mathbf{E} \tag{1.8}$$

where K is the unitless *dielectric constant* or *relative permittivity* of the material, and ϵ_0 is the permittivity of free space with units of farads/meter.

$\mathbf{D}$ is related to the charge on the wire by Maxwell's equation

$$\nabla \cdot \mathbf{D} = \rho \tag{1.9}$$

Insulator	Dielectric Constant dimensionless	Breakdown Field V/meter	Loss Tangent dimensionless
Vacuum	1.0000		0
Air	1.0000		0
Silicon $100\Omega \cdot cm$	11.8	3×10^9	0.33
Silicon $10\Omega \cdot cm$	11.8	3×10^9	3.3
Silicon Dioxide	3.9	6×10^8	.00006
Silicon Nitride	7.5		
Silicon Carbide	42		
Diamond	5.7		
BeO	6.8		
AlN	8.8		
BN	6.5		
Polyimide	3.5		.01
Teflon	2.1		.00015
Alumina	9.4		.001
Glass Epoxy FR-4	4.1		.03
Epoxy-Kevlar	3.6		
Benzocyclobutene	2.6		
Water	80		
Glycerin	42		

Table 1.3: Dielectric Constants and Breakdown Fields for Important Insulators

which can be integrated across the bottom surface of the conductor to give the total wire charge as

$$Q = \int_A \rho = wl\rho = K\epsilon_0 wl(\frac{v}{h}). \tag{1.10}$$

Differentiating with respect to time, we arrive at the capacitive voltage current relationship

$$i = C\frac{dv}{dt} \tag{1.11}$$

where the capacitance of the parallel plate structure is given by the relationship

$$C = K\epsilon_0 \frac{wl}{h}. \tag{1.12}$$

Again, the capacitance is controlled by a material constant and a geometric factor.

Example:

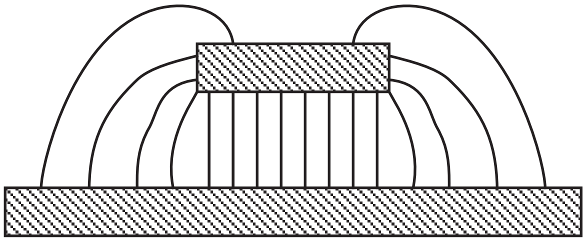

Figure 1.4: Electric Field Distribution Around the Prototypical Wire

> A printed circuit board 30 centimeters on a side is fabricated from epoxy-fiberglass. The power and ground signals are distributed on two internal power planes separated by five mils of board material. Edges and holes for components occupy 10% of the board area. Calculate the decoupling capacitance available between the power and ground planes due to the board construction.

Solution:

> The dielectric constant of the PC board material will be 4.2. The thickness is (.005 inches)(.0254 meters/inch) = 1.270×10^{-4} meters. The board area is .3 meters $\times$.3 meters or .09 square meters, less 10%, or .081 square meters of active area.
> The capacitance is

$$C = (4.2)(8.85 \times 10^{-12} F/m)(.081 m^2)/(1.27 \times 10^{-4} m) = 3.825 fF. \tag{1.13}$$

Example:

> A reverse biased silicon PN junction has a depletion layer thickness of one micron. Calculate the capacitance per square micron of the junction.

Solution:

$$C = (11.8)(8.85 \times 10^{-12} F/m)/(10^{-6} m) = 0.104 ff/\mu^2 \tag{1.14}$$

1.3.1 The Permittivity of Materials is not Constant

The use of the dielectric constant in describing materials is only a linear approximation to the behavior of real materials, although it is an extremely useful approximation. Real materials can exhibit quite complex behavior, with frequency dependent dielectric constants, anisotropic behavior which must be treated with tensor rather than vector techniques, and even hysteretic behavior producing permanent electric fields in electret structures. Fortunately, most insulators important in digital design can be well approximated by simple dielectric constants, although at the frequencies important in modern digital design a variety of materials used in constructing ceramic capacitors exhibit dramatically reduced dielectric constants.

1.3.2 Fringing Fields add an Important Capacitance

For wires with a width small compared to the height above a conductive plane, the formula 1.12 requires important corrections. The effective electrical width of a wire for the purposes of calculating capacitance is larger than the physical width of the wire. A common rule of thumb is that the effective wire width must be increased by $.75h$ to more accurately model total capacitance. Note that this implies that the capacitance versus width curve for a conductor decreases almost linearly until the width approaches the height of the conductor above the plane. It then remains nearly constant, independent of physical width.

Example:

> Calculate the total capacitance of a .5 micron wide aluminum wire crossing the length of a one centimeter silicon die. The metal wire is above a conducting silicon substrate, insulated by a 400 nm silicon dioxide insulator. Recalculate and compare the capacitances for metal widths of 1 and 2 microns.

Solution:

> Solution goes here.

1.3.3 Area and Perimeter Capacitance

The calculation of fringing fields is sometimes done by separately calculating the capacitance due to the area of the node, multiplying by the capacitance per unit area, and then adding to that area capacitance a fringing capacitance related to the extra capacitance at the edge of the structure. The fringing capacitance is calculated by multiplying by a perimeter capacitance given in units of capacitance per unit length.

1.3.4 The Fundamental Law of Digital Design

The v-i relationship for a capacitor is

$$i = C\frac{dv}{dt}. \tag{1.15}$$

We can rewrite this equation as a difference equation, and rearrange the terms to arrive at the *fundamental law of digital integrated design*,

$$\Delta t = \frac{C\Delta v}{i}. \tag{1.16}$$

Small integrated circuits are dominated by capacitive parasitics, and this simple relationship enumerates all of the ways to reduce delays in such circuits:

- Reduce the node capacitance
- Reduce the node voltage swing
- Increase the current available to charge the node.

Throughout the book, we will come back to this simple relationship for ideas on how to improve performance of digital integrated systems.

1.3.5 Power Dissipation and Capacitance

Power is not consumed within the capacitor when it is charged or discharged. Nonetheless, it is common to discuss power dissipation associated with capacitances. This is because when the capacitor voltage is charged by Δv through a resistive component, the total energy dissipated is independent of the resistor value, but is given by

$$W = \frac{1}{2}C\Delta v^2. \tag{1.17}$$

If this capacitance is charged and discharged at a frequency f, then we arrive at the equation expressing the most important source of power dissipation in modern digital systems:

$$P = C\Delta v^2 f. \tag{1.18}$$

The resistance and capacitance affect the power by controlling the maximum speed at which a system can be cycled, related to the RC time constant. The capacitance controls the energy dissipated during each cycle. Reducing the resistance makes the potential operation speed of the system higher, enabling a higher f.

The energy dissipation associated with capacitive loads is not inevitable, because it occurs not within the capacitor, but within the resistances driving the capacitor. Clever circuit techniques can be used to recover nearly all of the capacitive energy which would otherwise be dissipated, and are an active area of research.

1.3.6 Capacitances Fall under Device Scaling

The capacitance of a wiring node under scaling is given by

$$C' = K\epsilon_0 \frac{(w/k)(l/k)}{(h/k)} = K\epsilon_0 \frac{wl}{hk} = C/k. \tag{1.19}$$

Unlike resistance, the capacitance of nodes in a scaled system decreases, improving the expected performance.

Recall that the scaling behavior of resistive wires was an increase of the resistance by the same scaling parameter k. For important wire parasitics in integrated systems, the RC time constants of wires remain constant under scaling. Since most other delays are reduced significantly under scaling, the presence of constant RC delays in wire interconnect becomes an increasing problem for highly scaled systems. As a mask designer, there is little that can be done about such delays, since the RC product is also independent of wire width, except for fringing capacitance effects.

The RC wire delay in a given process technology is proportional to the square of the wire length, since both the total resistance and the total capacitance of the wire increase linearly with the length.

Problem:

> The Intel 2147 memory chip contains polysilicon select lines which are 4 mm. long fabricated in a process with a sheet resistance of 70 ohms per square. The area capacitance of these select wires consists of two parts. In the region of the integrated circuit where the polysilicon acts as a wire (the *field* region), the oxide under the wire is 800 nm thick. In the region where the polysilicon wire forms a transistor, the oxide thickness is 25 nm. Explain, using the RC model developed in the text, why the mask designer of the 2147 has expanded the width of the select lines in the field region of the integrated circuit.

Solution:

> We can estimate the RC constant of the wire

1.3.7 Capacitive Coupling between Nodes is Important

1.4 Inductance

The final parasitic wiring component is *inductance*. We can determine the wiring inductance following a similar derivation to that of our capacitance extraction. Again we assume in this discussion that h is small compared with

w. Assume that the wire shown in Figure 1.1 carries a current of i amperes. The resulting magnetic field intensity can be determined from the equation

$$i = \oint \mathbf{H} \cdot dl, \tag{1.20}$$

relating the line integral of the field intensity around the conductor with the current through the conductor. The $\mathbf{H}$ field intensity is small outside of the region between the wire and the ground plane, and can be approximated as zero. The integral then simplifies to

$$i = w\mathbf{H}_0, \tag{1.21}$$

where $\mathbf{H}_0$ is the approximately constant $\mathbf{H}$ field between the conductor and the ground plane.

The flux density is related to the field intensity by the material relationship

$$\mathbf{B} = \mu\mathbf{H} = M\mu_0\mathbf{H}, \tag{1.22}$$

where M is the dimensionless relative permeability and μ_0 is the permeability of free space, $4\pi \times 10^{-7}$ henry/meter.

Combining these equations, and differentiating with respect to time, we arrive at

$$\frac{\partial \mathbf{B}_0}{\partial t} = M\mu_0 \frac{1}{w}\frac{di}{dt}. \tag{1.23}$$

Applying Maxwell's equation

$$\oint \mathbf{E} \cdot dl = -\int_S \frac{\partial \mathbf{B}}{\partial t} \cdot dS \tag{1.24}$$

to the boundary dl along the length of the wire and returning along the ground plane, the line integral becomes the voltage change along the wire, and the surface integral becomes multiplication by hl. Thus, we obtain the device equation for an inductor,

$$v = M\mu_0 \frac{hl}{w}\frac{di}{dt} = L\frac{di}{dt}, \tag{1.25}$$

where the inductance L has a value

$$L = M\mu_0 \frac{hl}{w}. \tag{1.26}$$

Again, the inductance depends on material properties and a geometric factor.

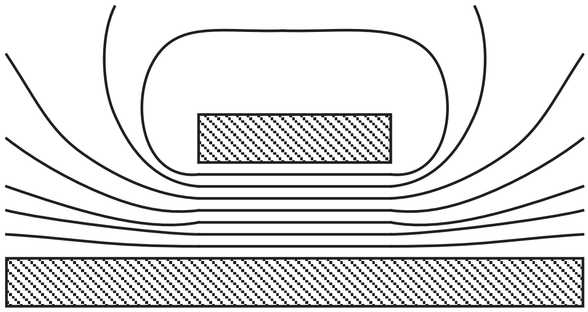

Figure 1.5: Magnetic field Distribution around the Typical Wire

1.4.1 Permeability of Materials

Many important magnetic materials have a highly nonlinear and hysteretic relationship between field intensity and flux density; for the discussion of wiring, we consider here only the linear materials. Almost all important insulating materials, indeed, have a relative permeability, M, of very nearly 1. High relative permeability effects become important in ferromagnetic transformer core windings, which are rare in digital and integrated circuit applications.

1.4.2 Scaling of Inductance

An analysis of inductance scaling is very similar to the capacitance scaling derivation,

$$L' = M\mu_0 \frac{(h/k)(l/k)}{(w/k)} = L/k, \tag{1.27}$$

with the inductance falling with the scaling factor.

1.4.3 Inductance is Less Important in CMOS Digital Circuits

Capacitance is typically a first order concern in the design of integrated circuits, but little attention is paid to the inductance of on chip or on board wiring. The reasons for this concern are well placed, because the output impedance of a typical CMOS logic gate driving the wiring is thousands of ohms. The RC time constant clearly dominates the L/R time constant for output resistances in this range. The situation can be quite different in other logic families, such as Josephson Junction (JJ) logic, where the basic gate has an output resistance near zero. In JJ circuits, inductance is the major wiring parasitic, rather than capacitance.

1.4.4 Fringing Effects are Important

1.4.5 Coupling Inductance is Important

1.5 Resistive Capacitive Lines

The combination of more than one parasitic wiring component yields important behavior. The simplest of these combinations, the resistive capacitive line, is of first order importance in the design of modern integrated circuits, because of the relatively poor scaling behavior of wiring resistance. As we will see in future chapters, the performance of digital integrated devices increases with the scaling parameter k, while the performance of the wiring remains constant.

If we simply calculate the expected RC delay of a small wire, however, the delay naively is given by

$$RC = \rho \frac{l}{tw} K\epsilon_0 \frac{wl}{h} = K\epsilon_0 \rho \frac{l^2}{ht}. \tag{1.28}$$

Several important properties are immediately apparent. First, the delay is independent of the wire width, meaning that layout engineers have little or no control over the properties of the line by changing layout.

Second, the delay depends on the square of the wire length, dramatically penalizing long wire runs.

Finally, the scaling of the RC delay is unchanged,

$$(RC)' = Rk \cdot C/k = RC, \tag{1.29}$$

which results in the wiring component of delays in scaled integrated systems becoming an increasingly significant component of system delay.

Intuitively, we can think of the RC line as a series of RC lowpass filters, which effectively filter out all high frequency components from input signals. Since high frequency components carry the information in high speed digital systems, the removal of the high frequency signal components dramatically slows the maximum signalling rate.

A more careful analysis of the resistive capacitive line takes into acount the distributed nature of the components. Consider the line shown in figure 1.6, where we examine in detail two differential length sections of such a line, each of length δx. It is useful to rewrite all of the device parasitic component values in terms of their value per unit length:

$$\begin{aligned} \mathcal{R} &= \frac{\rho}{tw} \\ \mathcal{C} &= K\epsilon_0 \frac{w}{h} \\ \mathcal{L} &= M\mu_0 \frac{h}{w}. \end{aligned} \tag{1.30}$$

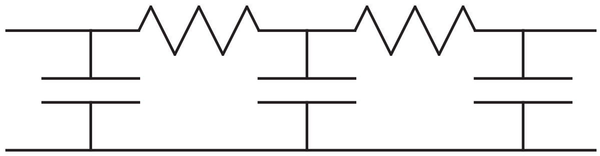

Figure 1.6: Differential Model for an RC Line

The per section resistance is then $\mathcal{R}\delta x$, and the capacitance, $\mathcal{C}\delta x$.

We assign voltages V_-, V_0, and V_+, to the left, center, and right nodes respectively, and write charge conservation for node V_0,

$$\frac{(V_- - V_0)}{\mathcal{R}\delta x} = \frac{(V_0 - V_+)}{\mathcal{R}\delta x} + \mathcal{C}\delta x \frac{dV_0}{dt}. \tag{1.31}$$

Taking the limit as δx approaches zero, we arrive at the governing equation for the resistive capacitive line,

$$\frac{\partial^2 V}{\partial x^2} = \mathcal{R}\mathcal{C}\frac{\partial V}{\partial t}. \tag{1.32}$$

This equation is the *diffusion equation* or the *heat equation*, and is also the governing equation for the temperature distribution along a thermally conductive rod. The unit voltage step response for a semi-infinite RC line is

$$V(x,t) = \operatorname{erfc}\sqrt{\frac{\mathcal{R}\mathcal{C}x^2}{4t}} = 1 - \operatorname{erf}\sqrt{\frac{\mathcal{R}\mathcal{C}x^2}{4t}}, \tag{1.33}$$

where erf is the error function, defined by

$$\operatorname{erf}(z) = \frac{2}{\sqrt{\pi}}\int_0^z e^{-\xi^2}\, d\xi. \tag{1.34}$$

The plot shown in figure 1.7 demonstrates the dramatic effect of distributed resistance and capacitance in long wires. The delay, again, is seen to depend on the square of the wire length, but we also note that the risetime of the signal is dramatically slowed for longer wires.

1.5.1 The Lumped Circuit Model

The partial differential equation model for the RC line is instructive, but difficult to work with in real applications. We can approximate the behavior of a distributed RC line quite well with much simpler models, such as the two or three section models of figure 1.8.

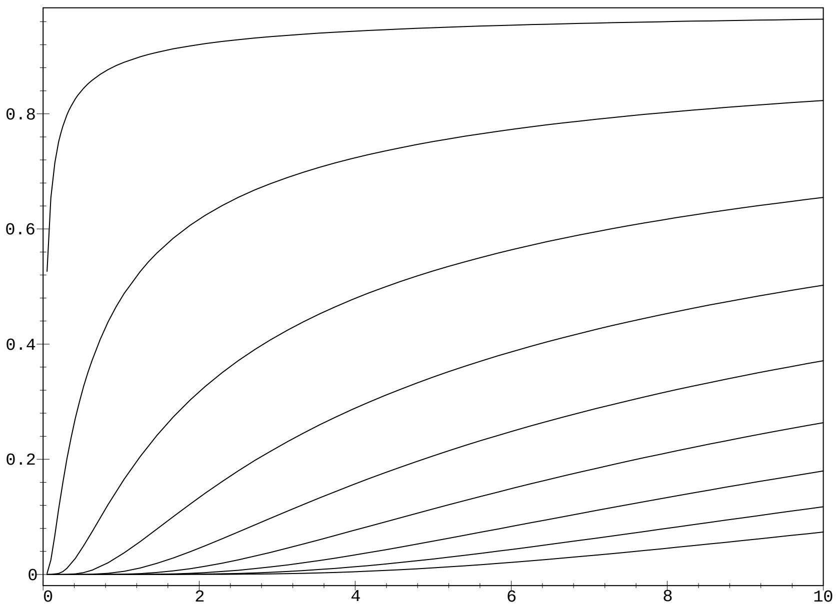

Figure 1.7: Voltage vs. time for an RC line at distances $n/\sqrt{\mathcal{RC}}$ for $n = 0.2, 1, 2, \ldots 8$.

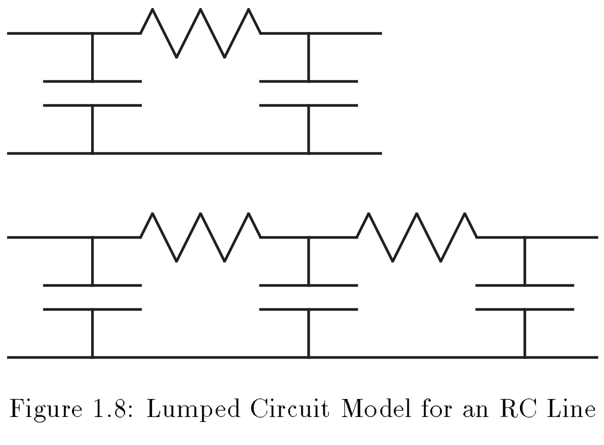

Figure 1.8: Lumped Circuit Model for an RC Line

1.5.2 When are RC Line Effects Important?

1.6 Inductive-Capacitive Transmission Lines

While RC wiring parasitics play the dominant role within CMOS circuits, at the macroscopic level, parasitic resistances are relatively low, and the dominant concern is the inductive capacitive (LC) wire parasitic.

Our second combined parasitic also yields important wire behavior. If we naively calculate the expected delay, τ, of the combined bulk components, the delay is estimated as

$$\tau = \sqrt{LC} = \sqrt{M\mu_0 \frac{hl}{w} K\epsilon_0 \frac{wl}{h}} = l\sqrt{MK\mu_0\epsilon_0}. \tag{1.35}$$

Several important effects are immediately apparent. First, the delay is linearly dependent on the wire length.

The signal has a constant propagation speed, which is given by

$$\nu = l/\tau = \frac{1}{\sqrt{\mathcal{LC}}} = \frac{l}{\sqrt{LC}} = \frac{1}{\sqrt{MK\mu_0\epsilon_0}} = \frac{c}{\sqrt{MK}}, \tag{1.36}$$

where c is the speed of light in vacuum, a physical constant equal to $1/\sqrt{\mu_0\epsilon_0}$, of defined numerical value $2.997924580 \times 10^8 m/s$. Note that the speed of propagation depends only upon the permittivity and permeability of the material surrounding the wire, not on the wire geometry.

The delay of LC dominated wiring under scaling is favorable,

$$\tau' = \sqrt{L'C'} = \sqrt{(L/k)(C/k)} = \tau/k \tag{1.37}$$

.

A more careful analysis of LC wiring takes into account the distributed nature of the inductance and capacitance. Consider the two sections of an LC wire shown in figure 1.9, each of length δx. As in formula 1.31, we use the parasitic values per unit length to define the inductance, $\mathcal{L}\delta x$, and the capacitance, $\mathcal{C}\delta x$, for each section.

We assign voltages V_-, V_0, and V_+, to the left, center, and right nodes respectively, and write charge conservation for node V_0,

$$i_- = i_+ + \mathcal{C}\delta x \frac{dV_0}{dt}. \tag{1.38}$$

Taking the time derivative, we arrive at

$$\frac{di_-}{dt} - \frac{di_+}{dt} = \mathcal{C}\delta x \frac{d^2V_0}{dt^2}. \tag{1.39}$$

We can rewrite the inductor vi relationship 1.25 as

$$\frac{di}{dt} = \frac{v_L}{\mathcal{L}\delta x}, \tag{1.40}$$

Figure 1.9: Differential Length Model for an LC Line

and substitute, arriving at

$$\frac{(V_- - V_0)}{\mathcal{L}\delta x} - \frac{(V_0 - V_+)}{\mathcal{L}\delta x} = \mathcal{C}\delta x \frac{d^2 V_0}{dt^2}. \tag{1.41}$$

Taking the limit as δx approaches zero, we arrive at the governing equation for the inductive capacitive line,

$$\frac{\partial^2 V}{\partial x^2} = \mathcal{LC}\frac{\partial^2 V}{\partial t^2}. \tag{1.42}$$

This equation is the *wave equation* or *telegrapher's equation.*

1.6.1 Solutions to the Wave Equation

The solutions to the wave equation consist of arbitrary function F

$$V(x,t) = F(\xi) = F(t - x/\nu) \tag{1.43}$$

We take the second derivatives of $V(x,t)$ with respect to x and t:

$$\begin{array}{ccccc}
\frac{\partial V(x,t)}{\partial x} & = & \frac{\partial F}{\partial \xi}\frac{\partial \xi}{\partial x} & = & -\frac{1}{\nu}\frac{\partial F}{\partial \xi} \\
\frac{\partial V(x,t)}{\partial t} & = & \frac{\partial F}{\partial \xi}\frac{\partial \xi}{\partial t} & = & \frac{\partial F}{\partial \xi} \\
\frac{\partial^2 V(x,t)}{\partial x^2} & = & -\frac{1}{\nu}\frac{\partial^2 F}{\partial x \partial \xi}\frac{\partial \xi}{\partial x} & = & \frac{1}{\nu^2}\frac{\partial^2 F}{\partial \xi^2} \\
\frac{\partial^2 V(x,t)}{\partial t^2} & = & \frac{\partial^2 F}{\partial t \partial \xi}\frac{\partial \xi}{\partial x} & = & \frac{\partial^2 F}{\partial \xi^2}.
\end{array} \tag{1.44}$$

Substituting 1.43 and its derivatives 1.44 into the wave equation 1.42 gives

$$\frac{1}{\nu^2}\frac{\partial^2 F}{\partial \xi^2} = \mathcal{LC}\frac{\partial^2 F}{\partial \xi^2} \tag{1.45}$$

which is a valid solution under the condition that the velocity ν is given by

$$\nu = \pm \frac{1}{\sqrt{\mathcal{L}\mathcal{C}}}, \tag{1.46}$$

in agreement with 1.36 above.

The $\pm$ in the above equation is extremely important to note carefully. Solutions to the wave equation are allowed with either a positive or negative velocity along the line, reflecting the obvious $+x$ and $-x$ wire symmetry.

Signals on LC transmission lines thus fall into two classes, those travelling from left to right, and those travelling right to left. Within each of these classes, signals propagate at a fixed speed, ν, along the line, while the shape of the wqveform is unchanged.

Total solutions to the wave equation consist of superpositions of these solutions. In particular, an individual line may simultaneously support signals travelling in both directions.

1.6.2 Waves on a Semi-infinite LC Transmission Line

Assume we are given an infinitely long LC dominated wire, initially at rest, $V(x,t) = 0$ for $t < 0$. To the end of the wire, $x = 0$, we attach, at time $t = 0$, a voltage source of amplitude $f(t)$. To match boundary conditions at the left end of the line, a forward wave of the form $f(t - x/\nu)$ must propagate down the wire, at speed ν.

At any position x_0 along the wire, we observe the voltage $f(t - x_0/\nu)$ – a copy of the original signal, delayed by an amount x_0/ν, but undistorted and unchanged in amplitude.

1.6.3 Impedance of Transmission Lines

We may rewrite equation 1.40 in the form

$$\frac{\partial V}{\partial x} = -\mathcal{L}\frac{\partial I}{\partial t}. \tag{1.47}$$

The current associated with driving the semi-infinite line can be found by substituting our solution 1.43 into this equation, arriving at

$$-\mathcal{L}\frac{\partial I}{\partial t} = -\frac{1}{\nu}F'(t - \frac{x}{\nu}). \tag{1.48}$$

Integrating with respect to t, we obtain

$$I = \frac{1}{\mathcal{L}\nu}F(t - \frac{x}{\nu}) + g(x), \tag{1.49}$$

where the constant of integration $g(x)$ can be shown by substitution into 1.42 to be only a constant g_0, independent of time and position.

The ratio of the input voltage to the input current of the semi-infinite line, the input impedance, is given by

$$\frac{V}{I} = \frac{F(t - \frac{x}{\nu})}{\frac{1}{\mathcal{L}\nu} F(t - \frac{x}{\nu})} = \mathcal{L}\nu. \tag{1.50}$$

We label this *characteristic impedance* Z_0, with a value

$$Z_0 = \mathcal{L}\nu = \sqrt{\frac{\mathcal{L}}{\mathcal{C}}}. \tag{1.51}$$

The characteristic impedance has units of ohms, and is unchanged under scaling. Unlike the propagation speed, the characteristic impedance depends on both the geometry of the wire and on material properties as we can see from the formula for its value,

$$Z_0 = \sqrt{\frac{\mathcal{L}}{\mathcal{C}}} = \sqrt{\frac{M\mu_0 \frac{h}{w}}{K\epsilon_0 \frac{w}{h}}} = \frac{h}{w}\sqrt{\frac{M}{K}}\sqrt{\frac{\mu_0}{\epsilon_0}}. \tag{1.52}$$

The physical constant, $\sqrt{\mu_0/\epsilon_0}$ is the impedance of free space, 377 ohms. The impedance is unchanged by wire scaling.

1.6.4 An Infinite Transmission Line Behaves as a Resistor

From the standpoint of the input terminals, the semi-infinite transmission line thus behaves precisely as a resistor, whose resistance has a value Z_0. This is sometimes surprising in light of the fact that inductors and capacitors do not dissipate energy, while a resistor is required to convert electrical to thermal energy. The conflict can be resolved by realizing that in a semi-infinite line, the energy, while not dissipated, travels ever further in the $+x$ direction, and is effectively lost to the remainder of the electrical circuit.

Another implication of the resistive behavior of infinite lines is that we can simulate an infinite line with a resistor whose value equals Z_0. In particular, if we have a finite line, we can make this line behave as an infinite line by adding a *termination* to the end of the line in the form of a resistor across the line of value Z_0.

1.6.5 Impedance of the Backward Travelling Wave

The current flow associated with a backward propagating wave is travelling in the $-x$ direction, so the impedance $Z_0 = V/I$ will also be negative for such waves, while it is positive for forward propagating waves. It doesn't matter if you keep this sign as part of the impedance, and think of the backward wave as having negative impedance, or if keep the sign as the positive direction of the current for the backward propagating wave being in the $-x$ direction.

1.6.6 Reflection Coefficients and Terminations

Consider now the transmission line in figure ??, with impedance Z_0, terminated with a resistor of value R_t. We excite the initially idle line with a forward propagating wave $V_f(x,t)$, and write KCL at the termination end of the transmission line:

$$I_f = I_b + \frac{(V_f + V_b)}{R_t}, \tag{1.53}$$

where I_f and I_b are the instantaneous currents associated with the forward and backward solutions at the end of the line, and V_f and V_b the corresponding voltages.

Rewriting this equation in terms of the impedances,

$$\frac{V_f}{Z_0} = \frac{V_b}{Z_0} + \frac{(V_f + V_b)}{R_t}. \tag{1.54}$$

Solving this equation for V_b,

$$V_b = \frac{R_t - Z_0}{R_t + Z_0} V_f = \Gamma V_f, \tag{1.55}$$

where the *reflection coefficient*, Γ is given by

$$\Gamma = \frac{R_t - Z_0}{R_t + Z_0}. \tag{1.56}$$

We note that for resistive terminations, the backward propagating solution is given as a constant multiplied by the forward solution, where the constant, the reflection coefficient, is always in the range $-1 \leq \Gamma \leq 1$. Consistent with the discussion above, if $R_t = Z_0$, the reflection coefficient is zero, and there is no reflected wave.

When $R_t > Z_0$, the reflected wave is a positive multiple of the forward wave; for $R_t < Z_0$, negative.

1.6.7 The Open Circuited Line Reflects with $\Gamma = +1$

One important special case is the termination $R_t = \infty$, the case of the open circuited termination. Calculating Γ,

$$\Gamma = \frac{R_t - Z_0}{R_t + Z_0} = \frac{\infty}{\infty} = +1. \tag{1.57}$$

This tells us that the magnitude of the reflected wave is equal to that of the incident wave. One way of thinking about this is to consider the current flow associated with the forward solution. When this current arrives at the end of the line, there is no place for it to go but to travel backwards, forming a backward propagating wave of the same sign and magnitude as the forward wave.

If we examine the voltage on the line at several locations a, b, c, d as a function of time, we note an extremely important point: the waveform is identical to that of an infinite (or properly terminated) line during its initial period. The signal must propagate to the end of the line, be reflected, and come back prior to our observing any difference due to the value of the termination resistor.

1.6.8 The Short Circuited Line Reflects with $\Gamma = -1$

1.6.9 Limitations on our Transmission Line Model

1.6.10 Measuring Voltages on Transmission Lines

1.6.11 Time Domain Reflectometry

1.6.12 Practical Impedance Values are Between 10 and 200 Ohms

1.7 RLC Lines