Digital circuitry simulation

The CAM-8 architecture offers great flexibility and efficiency for the purpose of simulating digital circuitry. Unlike conventional cellular-automata architectures, where in order to go from point A to point B a signal has to step through all the intervening cells, in CAM-8 one can have “express” conveyor belts that can carry signals over a long distance in a single step.

In the current embodiment of the CAM-8 architecture, processors are time-shared between a large number of sites—we gave priority to flexibility over raw speed. However, once a circuit-simulation strategy has been successfully developed and evaluated on this platform, one can directly port it to a more dedicated, massively parallel implementation of the same architecture, more appropriate for the high-speed simulation of large circuits.

The figure on the left shows an 8-bit shift-register with linear feedback, used as a random-number generator, followed by an 8-to-1 multiplexer driven by a 3-bit binary counter. That on the right, a multistage hexadecimal counter with integral 7-segment display.