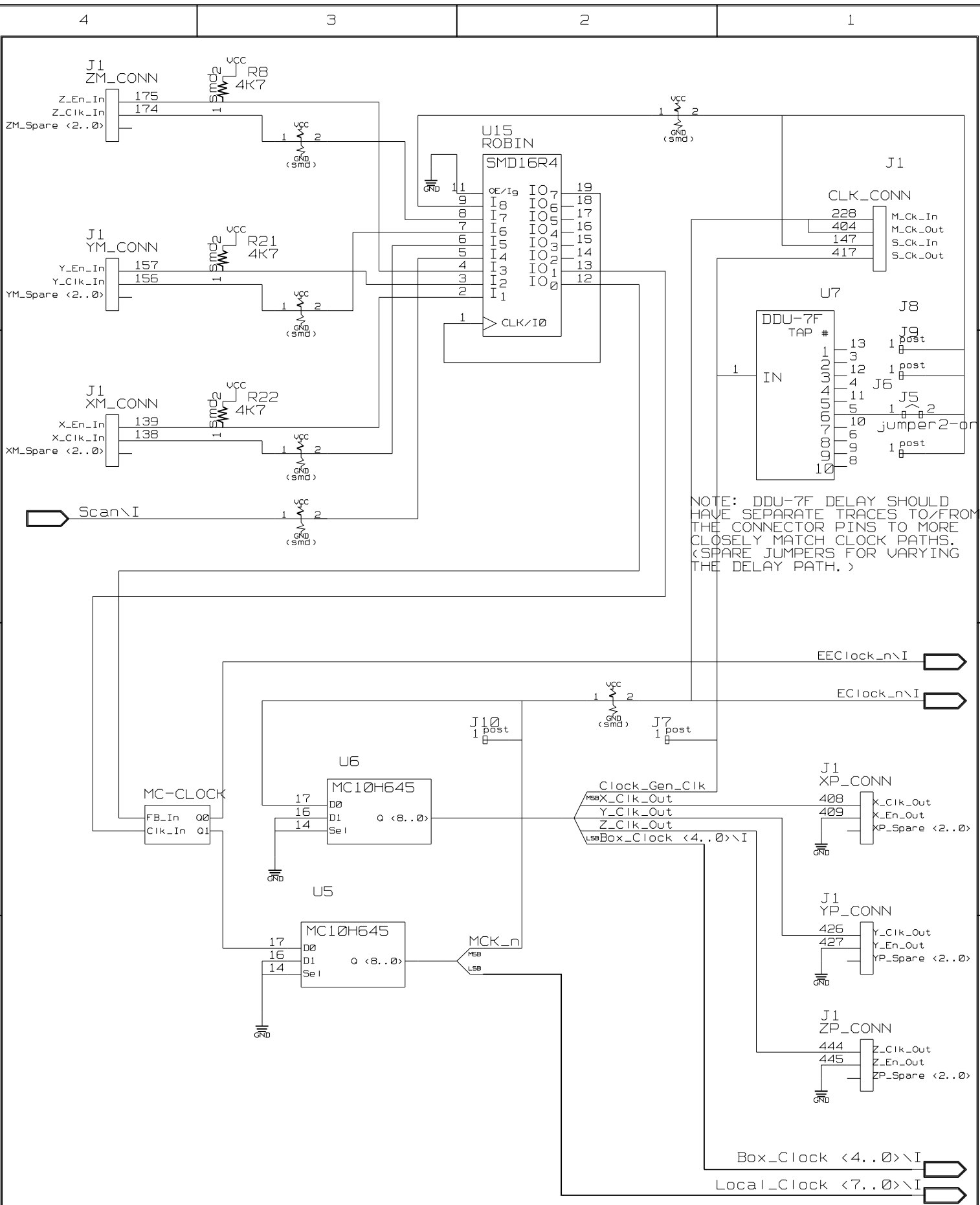
J1
ZM_CONN
Z_En_In
Z_Clk_In
ZM_Spare <2..0>
175
174
R8
4K7
J1
YM_CONN
Y_En_In
Y_Clk_In
YM_Spare <2..0>
157
156
R21
4K7
J1
XM_CONN
X_En_In
X_Clk_In
XM_Spare <2..0>
139
138
R22
4K7
Scan\I
VCC
GND
(smd)
U15
ROBIN
SMD16R4
OE/Ig
CLK/I0
J1
CLK_CONN
228
404
147
417
M_Ck_In
M_Ck_Out
S_Ck_In
S_Ck_Out
U7
DDU-7F
TAP #
IN
J8
J9
J6
J5
post
jumper2-on
NOTE: DDU-7F DELAY SHOULD HAVE SEPARATE TRACES TO/FROM THE CONNECTOR PINS TO MORE CLOSELY MATCH CLOCK PATHS. (SPARE JUMPERS FOR VARYING THE DELAY PATH.)
EEClock_n\I
EClock_n\I
J10
J7
U6
MC10H645
MC-CLOCK
FB_In
Clk_In
Q0
Q1
D0
D1
Sel
Q <8..0>
Clock_Gen_Clk
X_Clk_Out
Y_Clk_Out
Z_Clk_Out
Box_Clock <4..0>\I
MSB
LSB
J1
XP_CONN
408
409
X_Clk_Out
X_En_Out
XP_Spare <2..0>
U5
MCK_n
J1
YP_CONN
426
427
Y_Clk_Out
Y_En_Out
YP_Spare <2..0>
J1
ZP_CONN
444
445
Z_Clk_Out
Z_En_Out
ZP_Spare <2..0>
Box_Clock <4..0>\I
Local_Clock <7..0>\I
TITLE:
CLOCK_GEN
DRAWING
DATE:
Thu Feb 16 01:25:55 1995
ENGINEER:
Ken Streeter Frank Honore
PAGE: