ARTIFICIAL INTELLIGENCE LABORATORY

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

PHYSICS OF COMPUTATION SEMINAR

Date: Friday, May 7, 1999
Time: Talk at **11:00am**
Buffet lunch after the talk
(Vieri thesis defense follows at **2pm**)
Place: NE43, 8th-floor AI Playroom

Advanced Clock Powered Logic

Bill Athas
University of Southern California
Information Sciences Institute
`http://www.isi.edu/acmos`

In this seminar I will present Clock Powered Logic (CPL), which is a new low-power logic style for exploiting adiabatic charging in digital CMOS VLSI. Adiabatic charging reduces energy dissipation below the traditional $\frac{1}{2}CV^2$ limit by explicitly controlling the speed of energy transport between circuit nodes. In past and present forms, the practical means to exploiting adiabatic charging has been to tap the clock lines as a source of ac power.

CPL circuits are low power when used in conjunction with an energy-conserving clock driver. We have implemented two generations of experimental CMOS VLSI microprocessors based on CPL. In our experiments, the CPL designs were compared to conventional counterparts for frequency-versus-power performance. I will present simulation results and laboratory measurements which indicate that there can be a significant low-power advantage to CPL when used with a high-efficiency resonant clock source.

Host: Tom Knight

This talk is part of a seminar series on adapting computers and computations to the constraints of, and opportunities afforded by, microphysics; and on the development and application of the physical theory of computation and information. If you would like to receive electronic notice of these seminars, send email to "poc@mit.edu."