Clock-Powered CMOS: A Hybrid Adiabatic Logic Style for Energy-Efficient Computing

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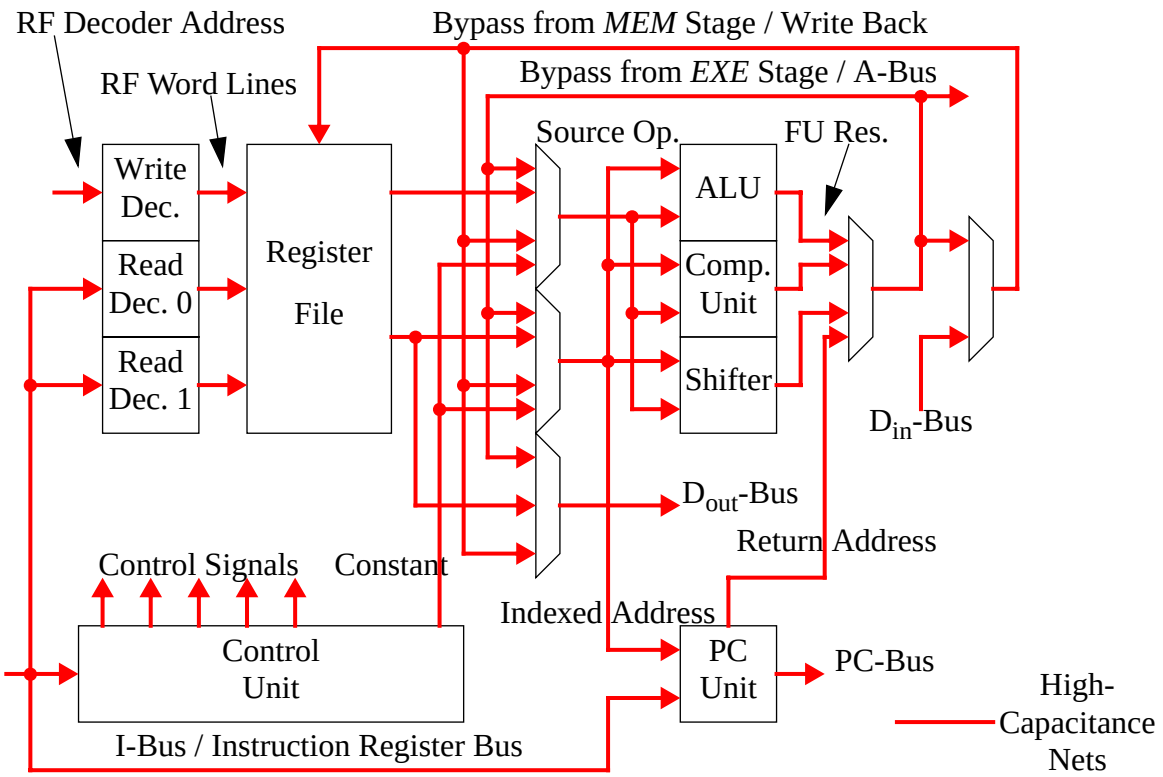
Outline

- The problem
- Standard approaches
- The idea of energy recovery and adiabatic charging
- Driver experiment
- Clock-powered logic
- Conclusions

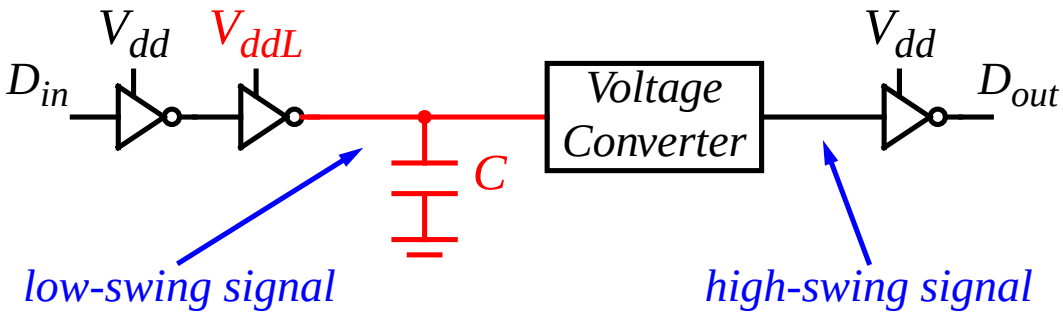
The Problem



- Processors contain some registers, a little bit of logic, and lots of long wires
- Problem: driving high-capacitance interconnects in an energy-efficient way

A Basic Approach

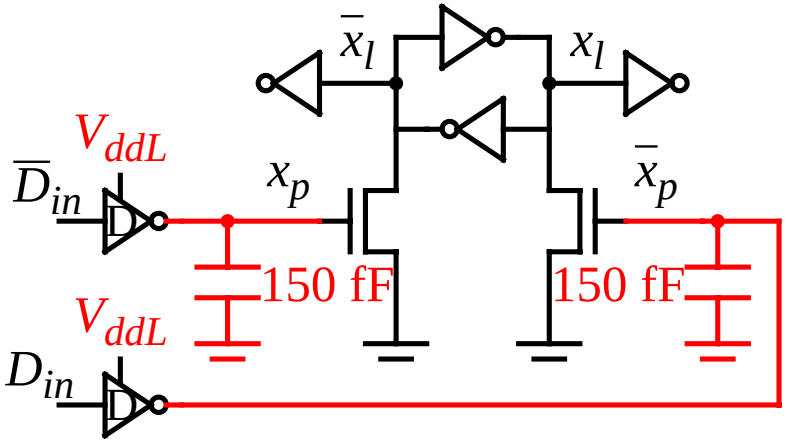
- The basic approach in CMOS:
  - Use reduced-voltage drivers and low-to-high voltage converters

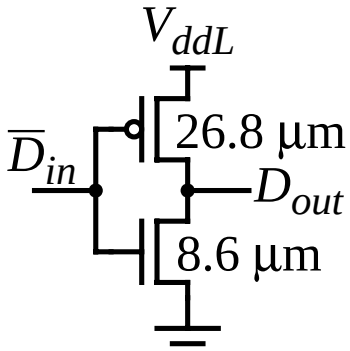


- Approach is limited by threshold voltages

Inverters as Low-Swing Drivers

- An inverter is used as a driver
- A dual-rail-input low-to-high voltage converter is used



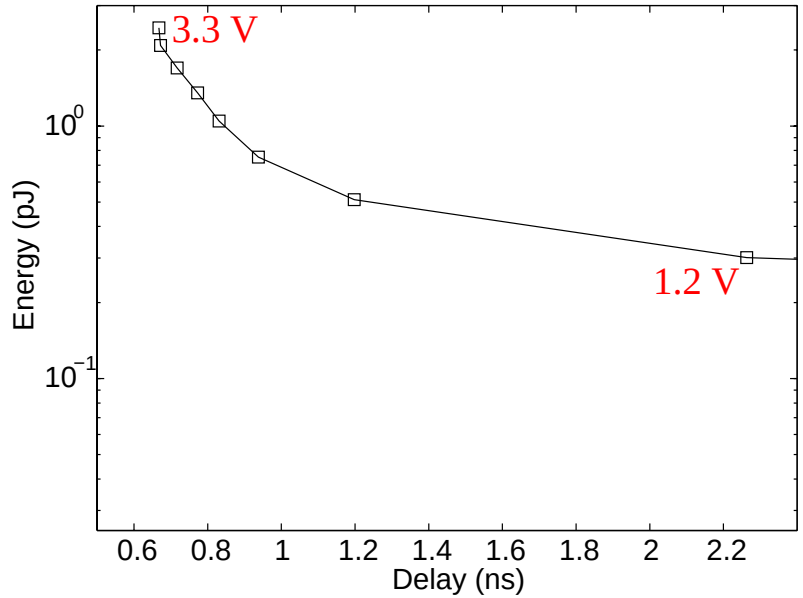


Driver

- HSPICE simulations for HP 0.5 µm, 3.3 V process

Energy vs. Delay for the Inverter

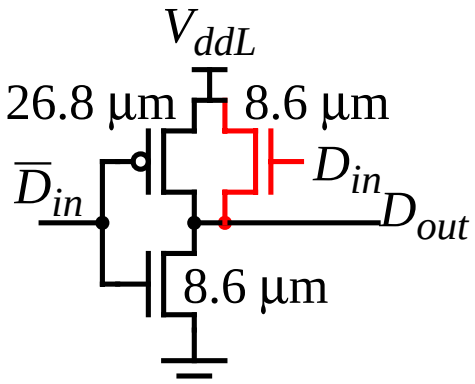
- V_{dd} is set to 3.3 V
- V_{ddL} is varied from 3.3 to 1.1 V
- Record energy for driving the load and delay through the converter



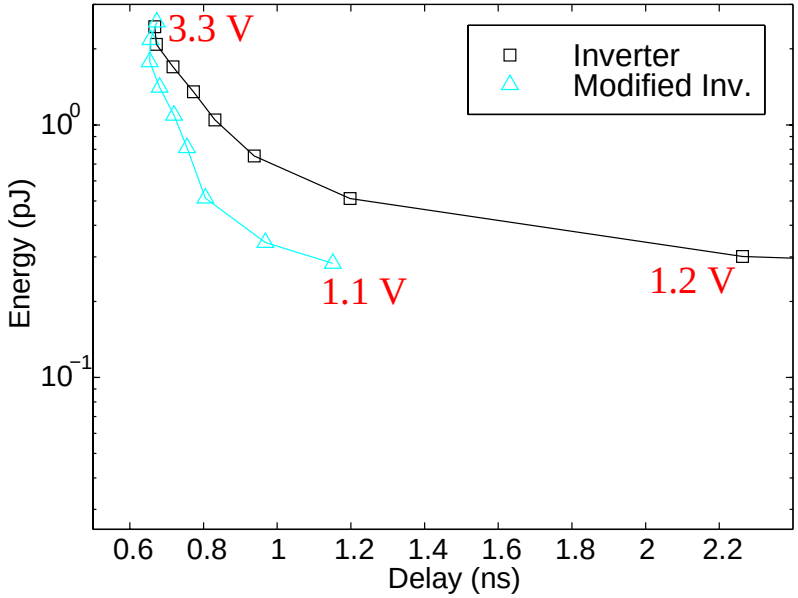
- Voltage reduction is limited by the threshold voltage of the converter
- Delay rapidly increases as V_{ddL} is scaled (3.6 ns for V_{ddL} = 1.1 V)

Simple Improvement

- A modified inverter is used as a driver

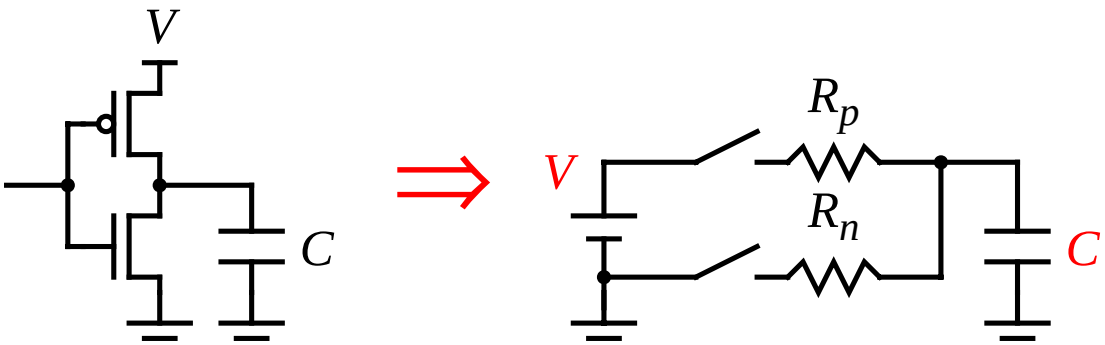


Modified Inverter



- Reduces delay for low voltages
- Minimum energy dissipation is still limited by the threshold voltage of the converter

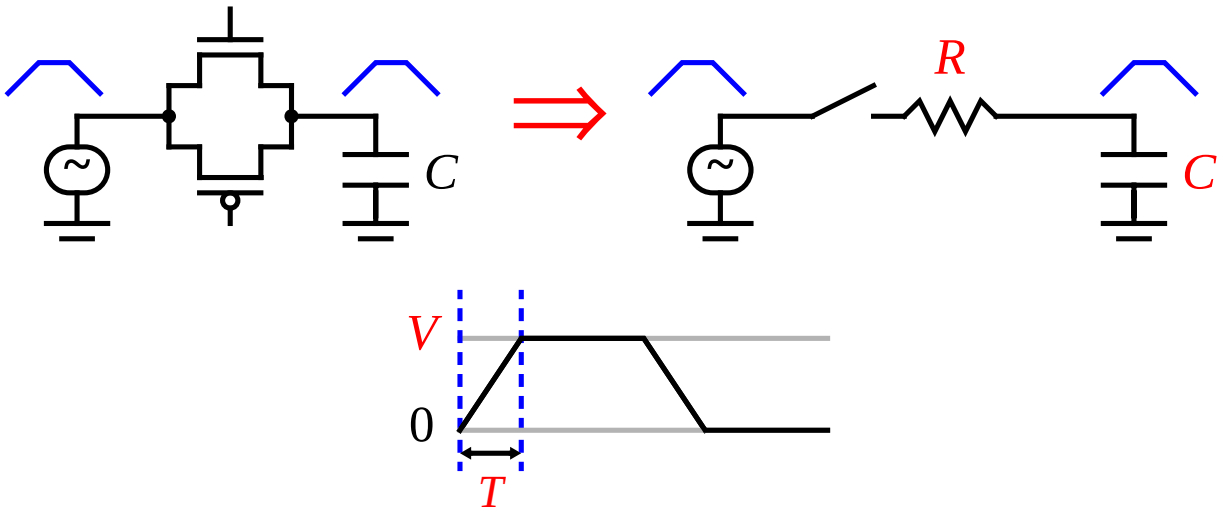
Standard CMOS



Standard CMOS: $E = CV^2$

- Possible ONLY to reduce voltage

Adiabatic Charging

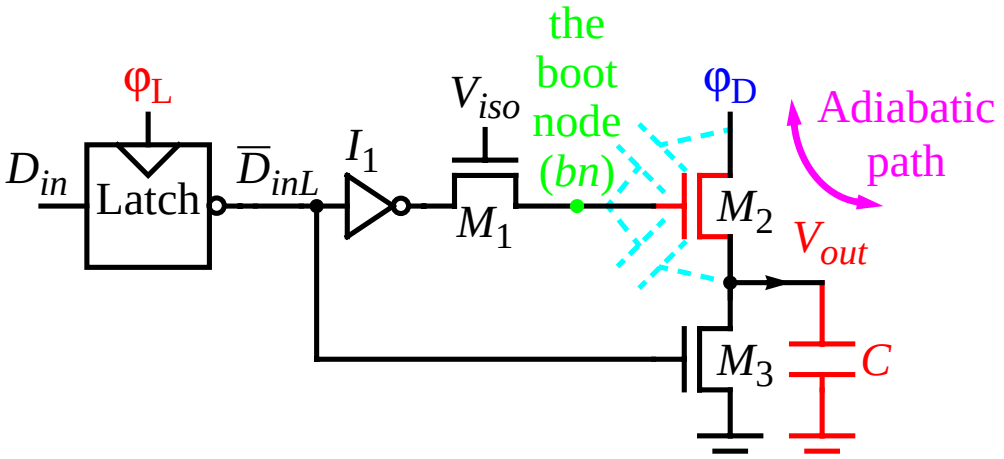


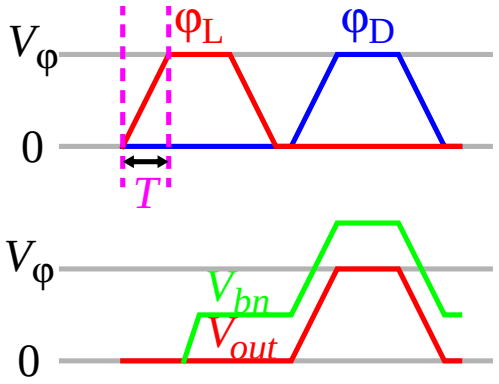
Adiabatic CMOS: $E = 2\frac{RC}{T}CV^2$

- Reduce dissipation by reducing voltage AND increasing the energy transport time

An Adiabatic Driver: The Energy-Recovery Latch

- Output node is clock powered
- Energy is injected and recovered through the same path
- Based on bootstrapped clocked buffer [Glasser & Dobberpuhl 1985]

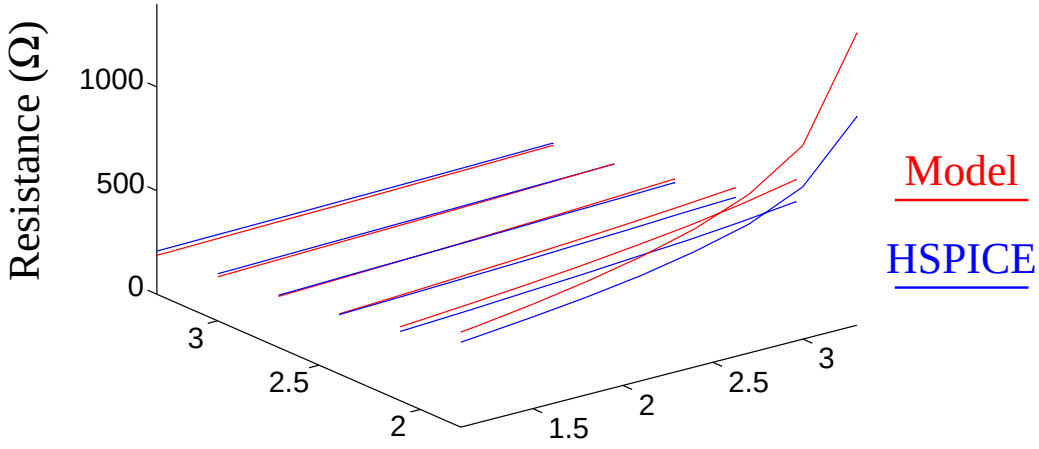




- Minimizes *R* for given boot-node capacitance
- Operates with two non-overlapping clock phases

Model for On-Resistance of Bootstrapped Transistor

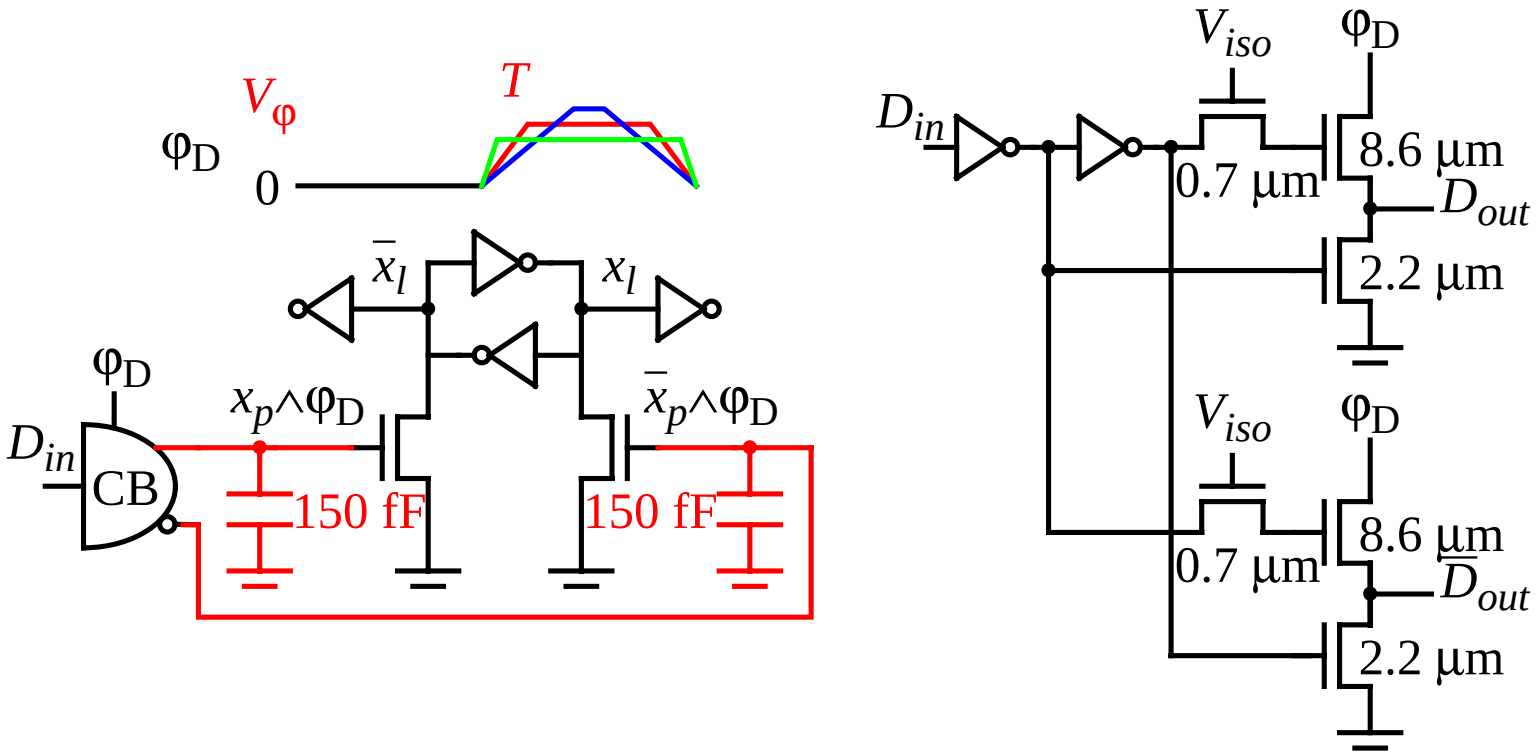
- Bootstrap nFET on-resistance was analytically modeled for the case of linear-ramp charging



- Analytical model can be used for sizing bootstrap transistor depending on load capacitance and switching time

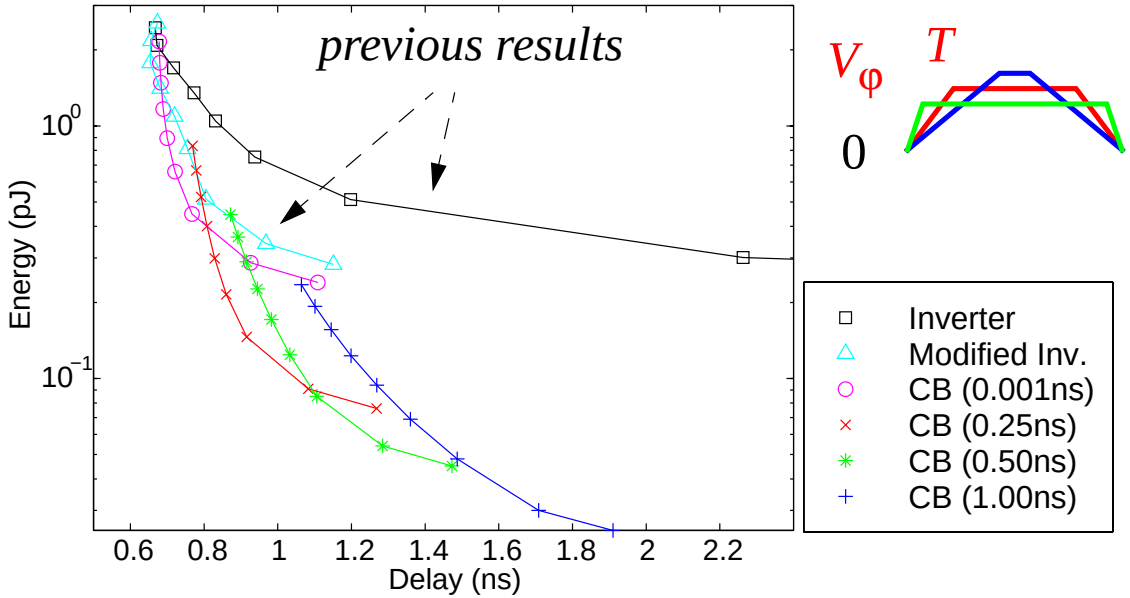
Driver Experiment Set-Up

- Purpose: to experimentally determine when increasing the switching time T is more energy efficient than reducing the clock voltage swing V_φ
- Voltage converter is inherently a pulse-to-level converter



Energy vs. Delay for all Drivers

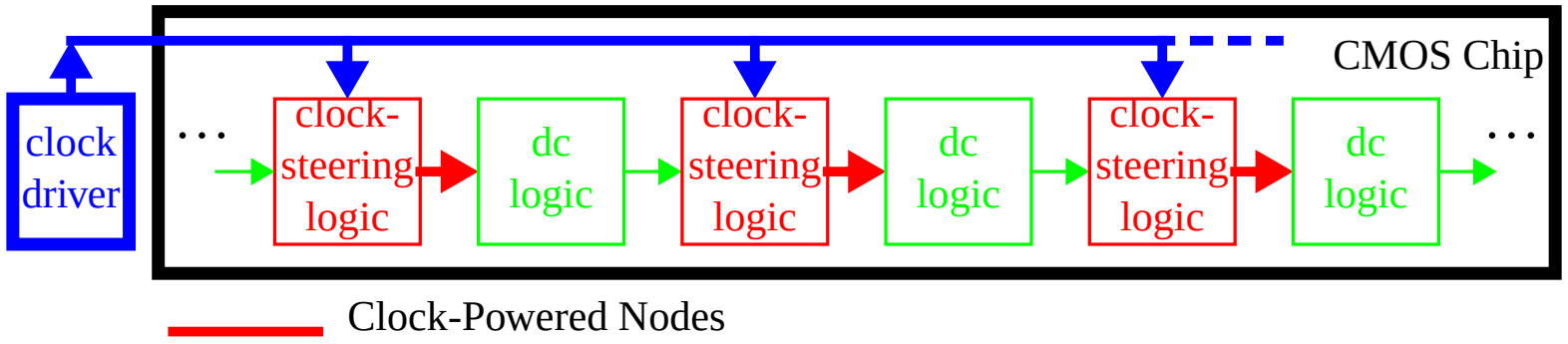
- Clock buffer: set V_φ (3.3-1.1 V) & T (0.001 ns, 0.25 ns, 0.5 ns, 1 ns)
- Conventional drivers: set V_{ddL} (3.3-1.1 V)
- Record energy for driving the load and delay through the converter



- Clock-powered approach has superior scalability because both clock voltage swing V_φ and switching time T can be varied

Clock-Powered Logic Design

- General approach:
  - Use the clock rails to inject and recover the energy
  - Derive as much operating power as possible from the clock rails
- General guidelines:
  - Need an efficient clock driver
  - Innovate in the design of a clock-steering logic
  - Use conventional precharged, pass-transistor, static logic
  - Use the clock-steering logic for high-capacitance loads



Clock-Powered Logic for Optimized Energy vs. Delay

- Reduce dissipation where dissipation is a problem
  - — Node-selective energy recovery
  - — Energy is recovered only from high-capacitance nodes
- clock-powered nodes: adiabatically switched
  - — "1": pulsed to a clock-voltage swing V_{φ}
  - — "0": clamped at 0 V
- dc-powered nodes: conventionally switched
  - — "1": pulled-up to a voltage V_{dd} from a dc supply
  - — "0": pulled-down to 0 V

The Energy Optimization Problem for Clock-Powered Logic

- Both clock-powered and dc-powered nodes contribute to energy dissipation
- The simplest expression that demonstrates the problem:

$$E = E_{cp} + E_{dc} \sim \frac{RC_{cp}}{T} C_{cp} V_{\varphi}^2 + C_{dc} V_{dd}^2$$

- $C_{cp} \gg C_{dc}$ for better energy efficiency
- Asymptotically E_{dc} dominates

Conclusions

- Clocked buffers offer better energy vs. delay scalability than reduced-voltage drivers
  - Energy depends on clock voltage swing and transition time
- Clock-powered logic is energy-efficient for implementing large-scale microsystems when:
  - the system can be partitioned into C_{cp} and C_{dc} with effectively $C_{cp} \gg C_{dc}$
  - long transition time of clock-powered nodes can be tolerated without changing overall system delay