MIT9904-04 Malleable Architectures for Adaptive Computing
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Project Overview

• TRS
  – High Level Architecture Specification Language and Synthesis

• Malleable Architectures
  – Arch. Specific ISA
  – Malleable Caches
Progress Through June 2000

• Column Cache Implementation
  – Dedicated SRAM for embedded applications
  – Partitioned Cache for real-time applications

• Adaptation Schemes for Multiprocessing

• Curious Caching
  – Initial Investigation
Research Plan for the Next Six Months

- Apply Technology to
  - Speech Processing (SLS)
  - Image Understanding
- Analyze Other Apps
- Architectural Description