

## MIT9904-04: Malleable Architectures for Adaptive Computing

MIT: Arvind, Larry Rudolph and Srinivas Devadas NTT: Hiroshi Sawada





- TRS
  - High Level Architecture Specification
    Language and Synthesis

Application

•Real-Time

Multimedia

Stream

- Malleable Architectures
  - Arch. Specific ISA
  - Malleable Caches





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## **Progress Through June 2001**

- Scheduler-based Prefetching
  - Process, Thread, Task



 Using Subband Processing to Improve Independent Component Analysis based Blind Source Separation



NTT - MIT Research Collaboration — Bi-Annual Report, January 1, 2001 – June 30, 2001



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**Research Plan for the Next Six Months** 

- Apply Speculative Memory Prefetching with
  - Column Caching
  - Custom Prefetch Engine Partitioning
- Analyze Other Apps
  - Event Driven Simulations
  - Speech Processing (SLS)
  - Image Understanding

