Project Overview

• TRS
  – High Level Architecture Specification Language and Synthesis
• Malleable Architectures
  – Arch. Specific ISA
  – Malleable Caches

Application
• Stream
• Real-Time
• Multimedia

Custom Embedded Microprocessor

ISA Specification
Cache Specification
TRS Compiler
Progress Through June 2001

- Scheduler-based Prefetching
  - Process, Thread, Task

- Using Subband Processing to Improve Independent Component Analysis based Blind Source Separation

Varying blocksize across subbands increases SNR by 27% over 512 sample blocksize!
Research Plan for the Next Six Months

• Apply Speculative Memory Prefetching with
  – Column Caching
  – Custom Prefetch Engine Partitioning

• Analyze Other Apps
  – Event Driven Simulations
  – Speech Processing (SLS)
  – Image Understanding