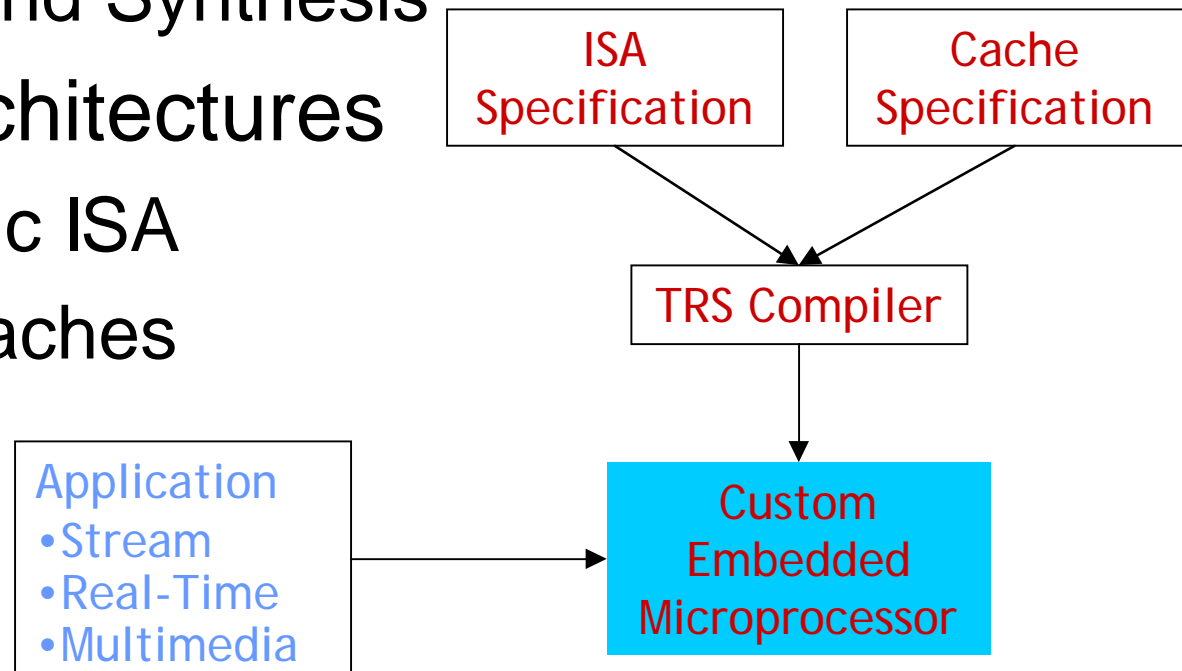




Project Overview

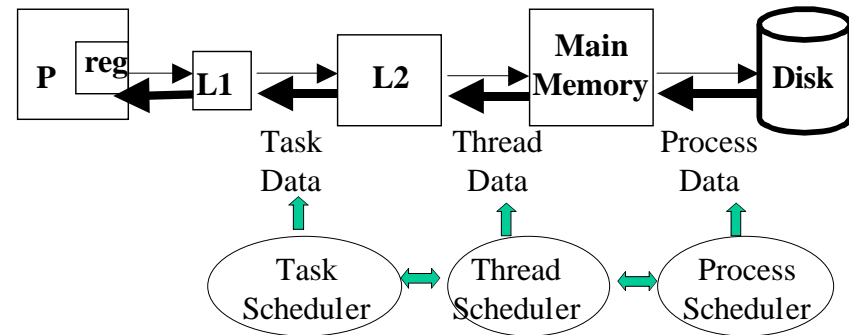
- TRS
 - High Level Architecture Specification Language and Synthesis
- Malleable Architectures
 - Arch. Specific ISA
 - Malleable Caches



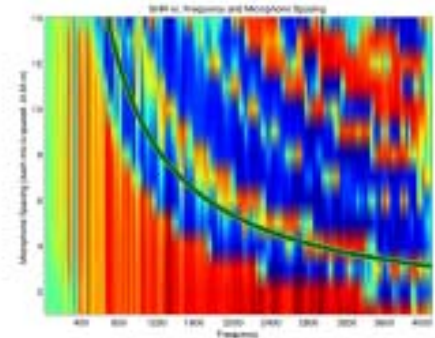
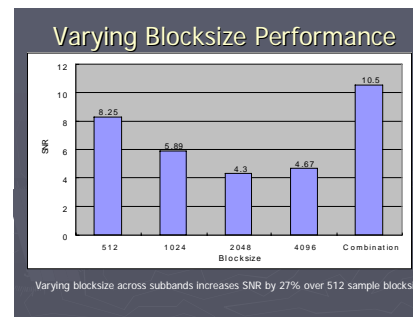


Progress Through June 2001

- Scheduler-based Prefetching
 - Process, Thread, Task



- Using Subband Processing to Improve Independent Component Analysis based Blind Source Separation





Research Plan for the Next Six Months

- Apply Speculative Memory Prefetching with
 - Column Caching
 - Custom Prefetch Engine Partitioning
- Analyze Other Apps
 - Event Driven Simulations
 - Speech Processing (SLS)
 - Image Understanding

