Project Overview

- TRS
  - High Level Architecture Specification Language and Synthesis
- Malleable Architectures
  - Arch. Specific ISA
  - Malleable Caches

Diagram:

- ISA Specification
- Cache Specification
- TRS Compiler
- Application
  - Stream
  - Real-Time
  - Multimedia
- Custom Embedded Microprocessor
**Cache Control**

- **Cache compression**
  - Apply data compression technique to L2 caches
  - Dynamically allocate the cache between compressed and uncompressed data
  - Improves performance & power consumption

- **Dynamic performance optimization**
  - Dynamic cache monitoring
    - Count marginal gains of each process for various cache sizes
  - Cache-Aware scheduling
    - Choose simultaneous processes to minimize cache contention
  - Cache partitioning
    - Manage cache allocation amongst processes

**Bandwidth Scheduling**

- Bandwidth requirement is bursty
  - Time-sharing: cold misses, difference among processes
- Make CPU schedule follow data (bandwidth) schedule
  - Prefetch for next job before starting the execution

![Diagram showing bandwidth scheduling and cache control](image)
Research Plan for the Next Six Months

• Apply Cache Compression to MPEG 2 & 3
  – Assume small cache, embedded processor
  – Show compressed cache behaves as if it was 2 to 4 times larger

• Apply Adaptive Prefetching to Stream-Based Computation
  – Show factor 2 reduction in required bandwidth
  – Show significant reduction in power requirements

• Microprocessor with Malleable Cache
  – Show performs as well as specialize network processor for routing applications.