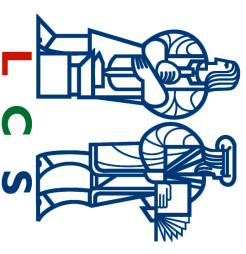


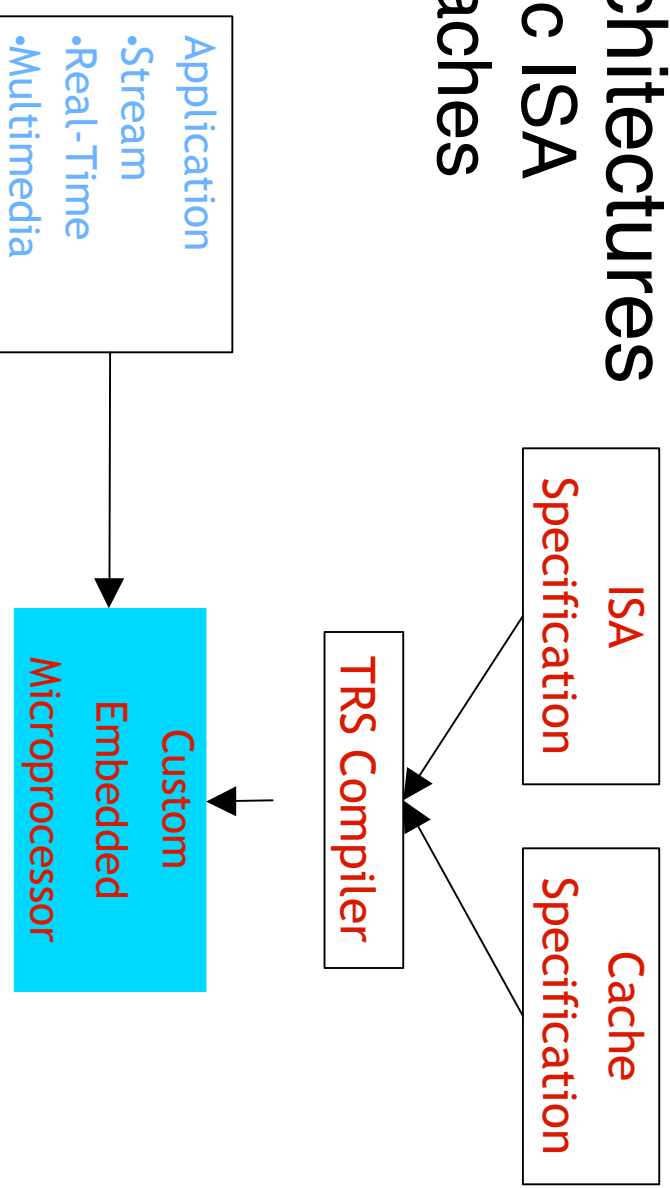
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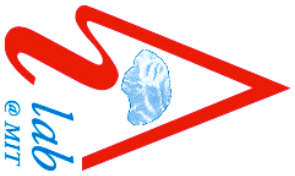
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Project Overview

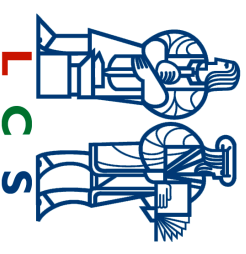
- TRS
 - High Level Architecture Specification Language and Synthesis
- Malleable Architectures
 - Arch. Specific ISA
 - Malleable Caches





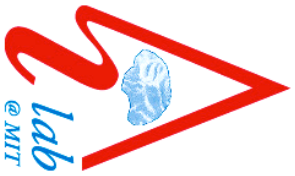
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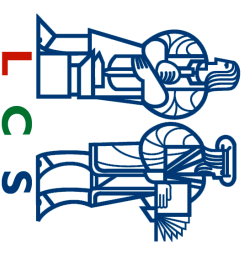
Progress Through June 2002

- Software-assisted cache replacement
 - Discover data in cache that can be “killed”
 - Modify replacement strategy to replace killed data before LRU data
 - Integrate modified replacement with a hardware prefetch method, where prefetched data is treated differently from normal data
- Next-job prefetching
 - Time-shared processes are scheduled by operating system
 - Prefetch next job’s data when current job is running
 - Emulated on IBM MXT (Memory Expansion Technology) system
 - Speedups obtained for streaming data applications



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Research Plan for the Next Six Months

- Study Machine Architecture for Stream Processing
 - Next generation applications (voice, video, sensors streams) demand new features from microprocessors
- Complete evaluation of adaptive prefetching on IBM MXT machine
 - Interactive applications such as web-servers
 - Compute-intensive benchmarks, including stream-based computations
- Investigate Memory Organization exploration for embedded designs
 - Partition on-chip embedded memory into cache and scratch-pad
 - Investigate methods to improve cache predictability