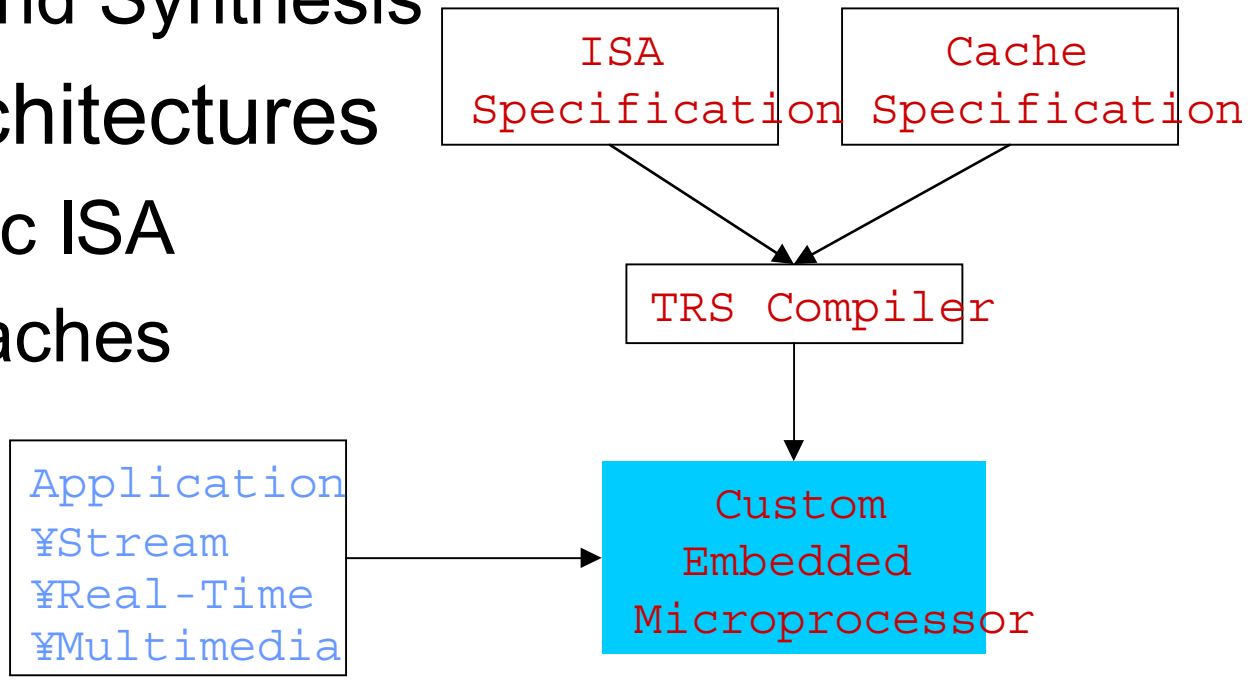
MIT: Arvind, Rudolph, Devadas NTT: Hiroshi Sawada

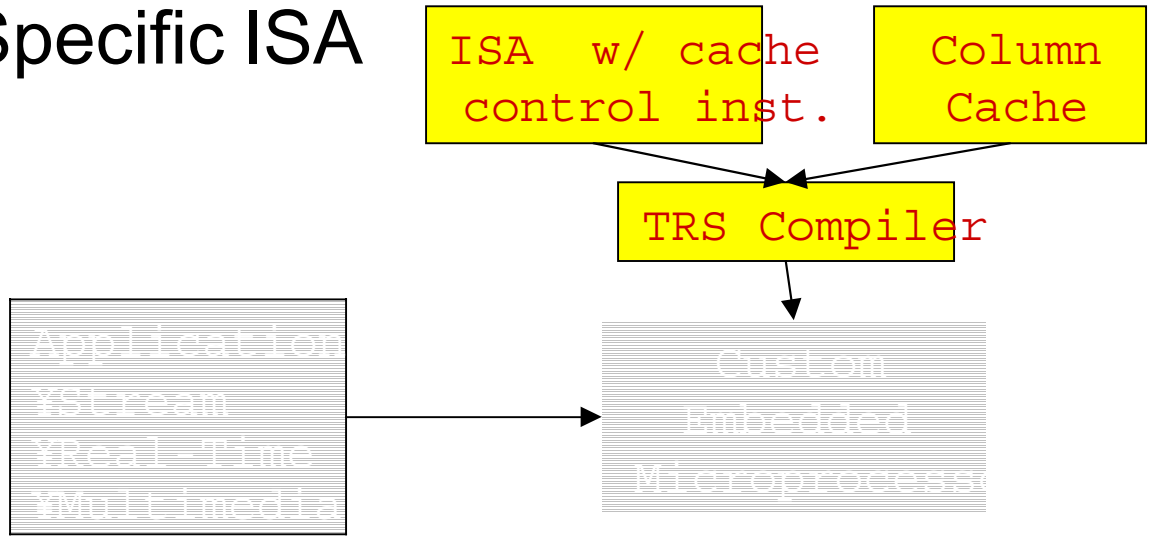
Project Overview

- TRS
  - High Level Architecture Specification Language and Synthesis
- Malleable Architectures
  - Arch. Specific ISA
  - Malleable Caches



Progress Through December 1999

- Prototype TRS Synthesis / Compiler
- Column Cache Implementation
  - Dedicated SRAM for embedded applications
  - Partitioned Cache for real-time applications
- An Application Specific ISA



Research Plan for the Next Six Months

- Apply Technology to
  - Embedded computing
  - Stream-based computations
  - Real-Time Applications