Project #: Malleable Architectures for Adaptive Computing

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**Project Overview**

- **TRS**
  - High Level Architecture Specification Language and Synthesis

- **Malleable Architectures**
  - Arch. Specific ISA
  - Malleable Caches
Progress Through December 1999

- Prototype TRS Synthesis / Compiler
- Column Cache Implementation
  - Dedicated SRAM for embedded applications
  - Partitioned Cache for real-time applications
- An Application Specific ISA
Research Plan for the Next Six Months

- Apply Technology to
  - Embedded computing
  - Stream-based computations
  - Real-Time Applications

Diagram:

- Application
  - Stream
  - Real-Time
  - Multimedia

ISA w/ cache control inst.

Column Cache

TRS Compile

Custom Embedded Microprocessor